AN/GYK-12

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CHAPTER 1

INTRODUCTION

1-1. Purpose

The purpose of this manual is to provide information pertaining to the operation, instructions, structure, and organization of the AN/GYK-12 (or L-3050) computer (hereinafter referred to as the computer) (see table 1-1). This manual, in conjunction with AN/GYK-12 Computer Assembly Language Reference Manual USACSCS-TF-4-2 or LSS User's Manual specification 137242-XXX provides programmers with information necessary to write programs for the computer.

This manual reflects minor differences between the TACFIRE, AN/TSQ-73, AN/TTC-39, and NICSTARE implementations. The differences are indicated at the appropriate places.

The major differences between the implementations are:

a. Input/Output Unit allocations.

b. Diagnose logic.

c. Front panel.

d. Instruction execution times.

For this reason the following sections of Chapter 4

III	Diagnose Features
IV	Front Panel and Maintenance
V	Peripheral Devices

and

Appendix A tables A-4 and A-5, Instruction Timing by Classes, reflect the specific implementation

NOTE

For the purpose of brevity, in certain places such as formats, the word "level" is used as an abbreviation of "program level" and the word "device" for "peripheral device".

1-2. Applicable Documents

This manual is a basic prerequisite for the following manuals concerning the AN/GYK-12 computer system.

TACFIRE

USACSCS-TF-4-2	AN/GYK-12 Computer Assembly Language Reference Manual
USACSCS-TF-4-1	TACPOL Reference Manual

AN/TSQ-73

137242-901	LSS (L-3050 Support Software) User's Manual

AN/TTC-39

137242-TBS	LSS (L-3050 Support Software) User's Manual for AN/TSQ-73

70061-401

1-3. Description

Chapter 1 specifies the purpose of the manual, the applicable documents, and provides descriptions of the various sections comprising this manual. Chapter 2 presents general information pertaining to the computer and consists of descriptions of the computer, computer organization, and the hardware sections comprising the computer. Chapter 3 discusses the memory communication characteristics and defines the program level concept. A detailed discussion of the special purpose registers is also included. Chapter 4 presents a discussion of the input/output (I/O) function of the computer. Chapter 5 presents general information pertaining to the data and instructions of the computer. Chapter 6 provides detailed descriptions of each of the computer instructions.

Table 1-1. Key Features of the AN/GYK-12 Computer

Category	Features
Computer Type	General-purpose; modular, with single or multiple central processing units.
Logic	Synchronous; silicon integrated circuits, HLTTL and TTL MSI.
Arithmetic Mode	Parallel; binary; fixed point.
Word Length	Memory word -- 32 bits plus parity bit; instruction word - 32 bits; data word - 64 bits, 32 bits, 16 bits, 8 bits, 1 bit.
Core Memory	8192-word assemblies modular expansion to 33.5 million words; overlapping memory cycles; two or four independent access ports; changeable bank address; memory protect by 2048-word block; one-microsecond access; less than 2.2 microseconds full cycle; wide temperature cores; power transient protection. Mass Core Memory Units (MCMU) of 131,072 words memory cycle, 2.5 μs.
Instructions	One hundred basic instructions; format contains command, mode, accumulator, index, and address.
Addressing	Single, half, and double word addresses; modifiable; full random addressing capability of 33.5 million words (1 billion bits); memory bus limited by line drive capability to maximum of 16 memory banks of two million-word size.
Address Modification	Nine modes: literal, direct, indirect, relative, with appropriate indexing; seven index registers.
Arithmetic	Sixteen accumulators for each program level; seven index registers for each program level, overlapped with accumulators; fixed-point binary arithmetic; numbers are signed integers, negative numbers are two's complement.
Programming	Sixty-four independent program levels with externally and internally activated priority-program-level switching and software override capability; dynamic priority hierarchy; 16 process registers for each program level to be used as accumulators, index registers, trap exits, mask registers, indicator flags; 16 memory page control and address registers for each program level; privilege and level link register for each program level; query register containing machine status indicators; linkage to executive program level; program activity register containing one status and one enable bit for each program level; multilevel priority interrupts; repeat - execute instructions from process registers; dynamic program relocatability using page/base address registers; program trap for each program level; call instructions; special diagnose and memory test instructions.
Data Handling	Byte instructions, logical operations; field, insert, shift, and comparison instruction.
Input/Output	Single word transfers; block transfers by bytes or words (asynchronous, independent of program execution); burst block transfers (synchronous with device); interleaved transfers from several devices; simultaneous I/O and instruction execution, independent I/O controller; automatic parity generating and device-dependent parity checking; read-write protection of I/O for 2048-word pages; separate normal and error termination for each device; alarm (clock) mode (for real-time clock); bootstrap program load.
Maintenance	Continuous system self-test; diagnostic instructions; bootstrap diagnostic; hang-up detectors for memory, central processing unit, I/O, real-time clock; automatic detection to gross function or module; modular construction.
Growth Capability	Directly addressable ram by CPU with protection; multiprocessor capability; optional time-of-day clock; optional floating point instructions; efficient use of 0.5 microsecond memory by CPU; sensing of discrete external stimuli; setting of discrete external functions.
Construction	Militarized, Transit Cases (convection cooling) or Rack mounted.

70061-1

CHAPTER 2

DESCRIPTION

Section I. AN/GYK-12 COMPUTER

2-1. Introduction

This section provides general information pertaining to the AN/GYK-12 computer. A discussion of the AN/GYK-12 computer organization and the main elements contained in the computer is presented.

2-2. The AN/GYK-12 Computer

The computer forms the nucleus of the AN/GYK-12 computer. The computer is a high-speed, general purpose, microelectronic digital computer. It makes use of the latest advances in circuits and packaging, in combination with an efficient system organization. The computer is a versatile machine with very extensive capabilities. This allows it to be efficiently and economically employed in a vast array of system applications, including the sophisticated and advanced real-time command and control system function. The characteristics of the computer are as follows:

a. Thirty-two bit instruction word.

b. One, eight, sixteen, thirty-two or sixty-four bit data word.

c. 2.0 microsecond memory read/write cycle.

d. Memory expandable in modular assemblies: banks consisting of 8192 words (four 2,048 word pages); or, the MCMU, consisting of 131,072 words. All memory words consist of 32 bits plus one parity bit, for a total of 33 bits.

e. Memory access control and protection, and internal parity checking.

f. One hundred basic instructions plus 50 extended mnemonic instructions.

g. Nine addressing mode combinations.

h. Sixty-four program levels.

i. Sixteen 32-bit multipurpose process registers and 18 additional special purpose registers per program level (all of the 16 process registers are useable as accumulators and seven are useable as index registers).

j. Four additional special purpose registers.

k. Up to 120 input/output channels each with program initiated but independently operating data transfers of up to 32 bits in parallel.

l. High input/output transfer rates of up to 300,000 thirty-two bit words per second on one channel or 180,000 thirty-two bit words per second when several channels are operating simultaneously. A queue word for each program level provides stacking of interrupts. (I/O data rate is dependent on memory speed.)

m. Automatic priority and high-speed multi-program switching.

n. Single or multiple processor configuration.

o. Compatible with the complete array of input/output devices, including the following:

(1) Other computers for direct couple or on line satellite use.

(2) Card and paper tape readers and punches.

(3) Printers.

(4) Tape drives.

(5) Drums.

(6) Discs.

(7) Displays.

(8) Remote input/output units.

(9) All types of displays and special purpose military and systems equipment and devices.

These features combine to give the computer impressive capabilities. These capabilities and how they function are explained in the text of this manual.

Section II. AN/GYK-12 COMPUTER ORGANIZATION

2-3. General

The AN/GYK-12 computer is a high-speed, general-purpose digital computer and contains three main elements; the central processing unit (CPU), the input/output unit (IOU), and the memory banks. The computer provides advanced features that are found in the most modern large scale computing systems. These features include: multiple program level control, memory expandability, multiple general purpose registers, and independently controlled input/output communication. Small size, light weight, and low power requirements are achieved by microelectronic integrated circuits. Militarized construction in transit cases (convection cooling) or rack mounted.

2-4. Central Processing Unit (CPU)

The central processing unit (CPU) of the computer is responsible for the arithmetic and control functions of the system. The functional block diagram shown in figure 2-1 illustrates the functional operation of the CPU. There are five major sections in the organization with communication among the sections carried on primarily via a data bus. The five major sections are as follows:

- Instruction controller
- Program level controller
- Arithmetic section
- Memory interface controller
- Process registers

The technique of communicating via the data bus minimizes the number of connections between blocks shown in figure 2-1. This technique has the effect of shortening the signal line lengths, thus reducing propagation delays and decreasing susceptibility to noise.

a. *Instruction Controller.* The instruction controller (see figure 2-1) controls the sequence of operations within the CPU and contains the indicator register and the instruction location register. The indicator register contains flags which indicate the program status of the data processing system. The instruction location register keeps track of the current instruction address.

b. *Program Level Controller.* The program level controller (see figure 2-1) contains the logic which controls the operation of one of the key real-time features in the computer. It is within the program level controller that the registers which represent the priority queue are updated and checked to determine whether the highest priority program available to be run is actually running. In addition, the control for switching program levels is contained in the program level controller.

c. *Arithmetic Section.* The arithmetic section (see figure 2-1) contains a high-speed 32-bit parallel adder as well as field extraction and alignment logic which make possible the variable field operations of the computer system.

d. *Memory Interface Controller.* The memory interface controller (see figure 2-1) contains the memory address register and logic; memory data register and logic; page control and address registers and logic; bit, byte and half-word selection logic. The memory address and memory data registers are normally associated with a memory-CPU interface. The page control and address registers contain the 16-page addresses associated with the active program level. Each page address accesses up to 2048 thirty-two bit words. The pages may be ordered in any sequence, thereby providing extensive flexibility in the organization of program and data. The bit, byte and half-word selection logic is used to select regularized short fields for processing by the arithmetic section or for transfer to another block. This capability to directly select 1, 8, or 16 bits from a 32-bit word, complements the variable field capability of the arithmetic block and permits complete flexibility in the storage and processing of data files.

e. *Process Registers.* Sixteen 32-bit process registers (see figure 2-1) are available to the active level program. The process registers are held in 32 sixteen-bit random access integrated circuit packages which operate with a cycle time of 200 nanoseconds. These high-speed elements may be used as accumulators, index registers, or to hold instructions during the execution of program loops.

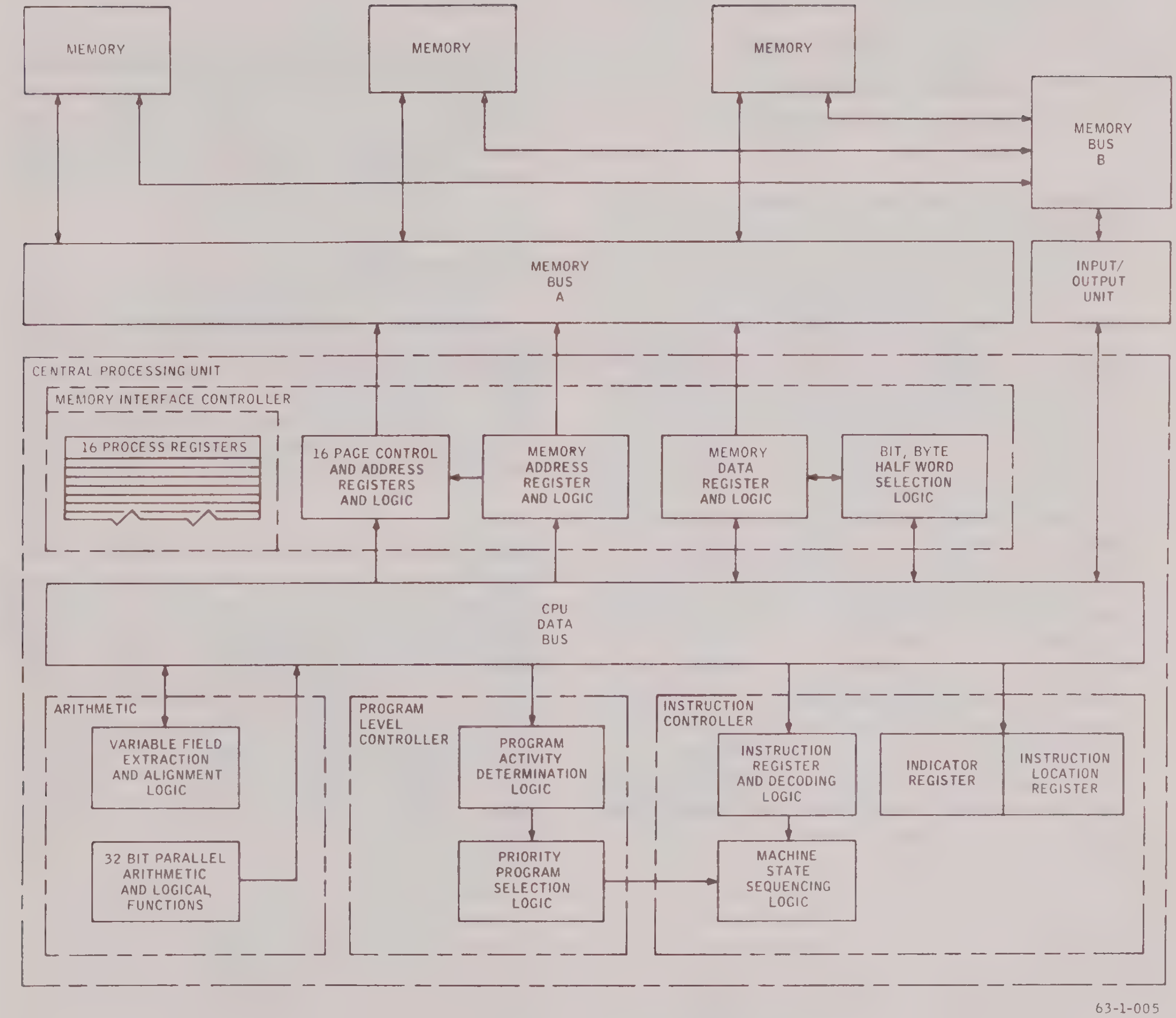

MEMORY
MEMORY
MEMORY
MEMORY BUS B
MEMORY BUS A
INPUT/ OUTPUT UNIT
CENTRAL PROCESSING UNIT
MEMORY INTERFACE CONTROLLER
16 PROCESS REGISTERS
16 PAGE CONTROL AND ADDRESS REGISTERS AND LOGIC
MEMORY ADDRESS REGISTER AND LOGIC
MEMORY DATA REGISTER AND LOGIC
BIT, BYTE HALF WORD SELECTION LOGIC
CPU DATA BUS
ARITHMETIC
VARIABLE FIELD EXTRACTION AND ALIGNMENT LOGIC
32 BIT PARALLEL ARITHMETIC AND LOGICAL FUNCTIONS
PROGRAM LEVEL CONTROLLER
PROGRAM ACTIVITY DETERMINATION LOGIC
PRIORITY PROGRAM SELECTION LOGIC
INSTRUCTION CONTROLLER
INSTRUCTION REGISTER AND DECODING LOGIC
MACHINE STATE SEQUENCING LOGIC
INDICATOR REGISTER
INSTRUCTION LOCATION REGISTER
63-1-005

Figure 2-1. AN/GYK-12 Computer Central Processing Unit Functional Block Diagram

2-5. Input/Output Unit (IOU)

The input/output unit (IOU), independent of the CPU, largely controls communication between the memory and the peripheral equipments. The IOU is comprised of the following sections:

- Input/Output controller (IOC).
- Front panel and maintenance.
- Input/output exchangers (IOX/IOE).
- Real-time clock.

The functional block diagram is shown in figure 2-2. A general discussion of the functional operation is presented in subsequent paragraphs.

a. *Input/Output Controller (IOC).* The IOC (see figure 2-2) receives its command from the keyword interpretation logic and from the CPU via the input/output (I/O) command interpretation logic. Either of these control sources controls the interface controls generation logic. Data transferred across the I/O DC bus is assembled or disassembled into words or bytes in the byte/word assembly-disassembly logic. The direct interface request for service from peripheral devices, or commands to devices, are transmitted by the device request/select logic. The priority/address determination logic and the memory addressing and control logic, control priority and memory addressing. The memory data interface logic administers the actual reading and recording of data in memory.

b. *Front Panel and Maintenance.* The function of the front panel and maintenance logic is to provide the format and display of internal memory and status control information from the IOU to the front panel.

c. *Input/Output Exchangers (IOX/IOE).* Data may be exchanged with peripheral devices either directly from the DC bus or through one of the IOX (see figure 2-2) which provide an AC long-line driving capability. Each IOX may have as many as eight independent peripheral devices attached to it. The IOE has the same function as the IOX but is used for short drive distances (50 feet).

d. *Real-Time Clock.* The real-time clock is included in the IOU merely for design convenience. Program cognizance of real-time passage is provided by the real-time clock. A primary function of this clock is to define the time-of-day or intervals of fixed or variable duration. Other functions are to monitor the responsiveness of IOU and program execution.

2-6. Memory Banks

The hardware implementation of the IOU is complete to the point that it operates almost in parallel with the CPU. The memory banks (see figure 2-2) reduce the probability of conflict for access between the CPU and the IOU. The memory banks store and read out information used by the computer. Memory banks may be the standard 8,192 word banks or the Mass Core Memory Unit (MCMU) with 131,072 words of memory per bank (33 bits per word).

Memory banks have typically two or four memory ports. Normally, one port is connected to the Central Processing Unit (CPU) and the other port to the Input/Output Unit (IOU). Other use of memory port(s) is application dependent and is usually defined in the system specification. For example, memory port(s) can be used for high speed data transfer between memory and indicated peripheral devices. This interface may be called Display Output Unit (DOU) in AN/TSQ-73, or Direct Memory Access (DMA) in AN/TTC-39 and NICS-TARE, or Direct Storage Access (DSA), or Selector Channel.

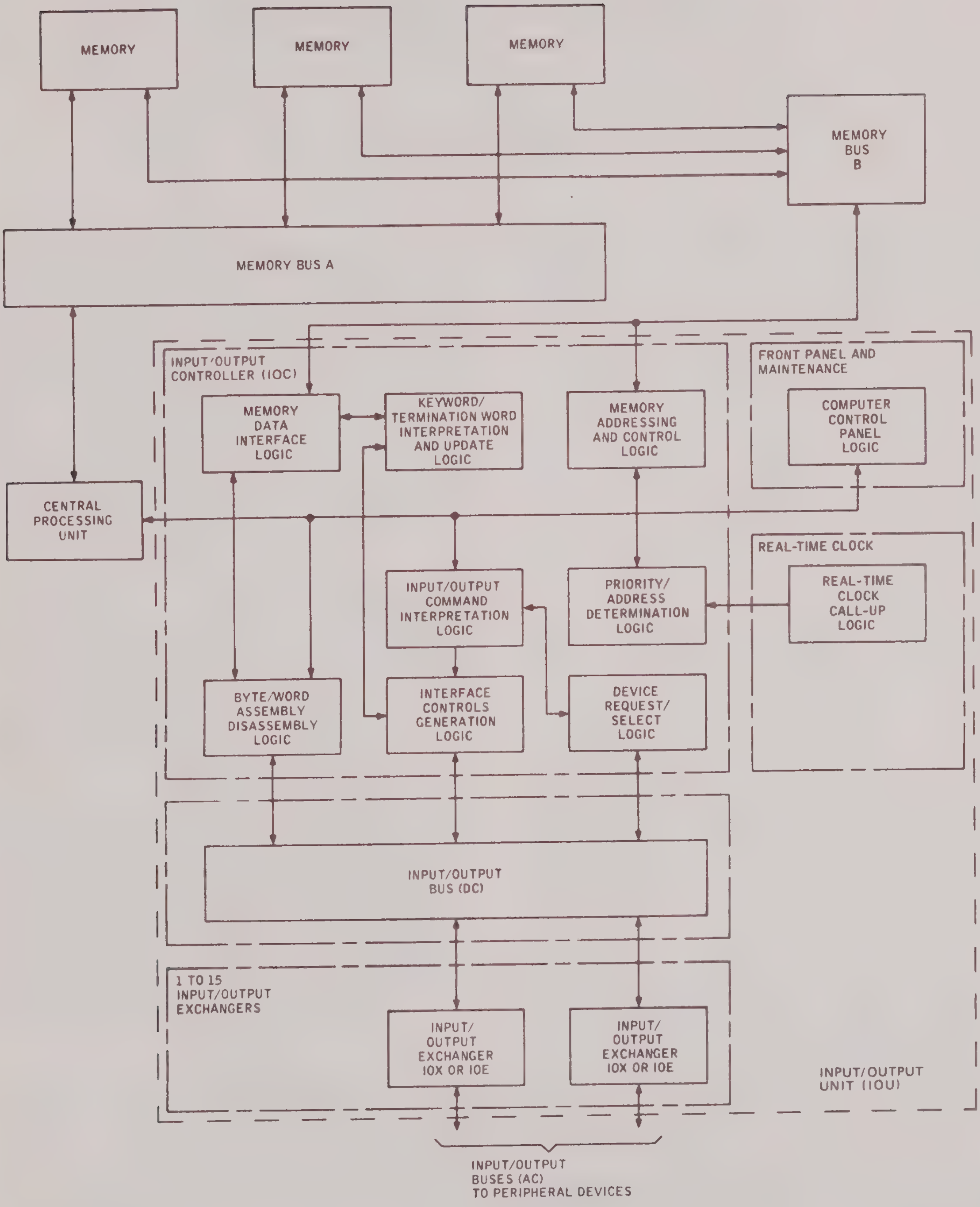

MEMORY
MEMORY
MEMORY
MEMORY BUS B
MEMORY BUS A
INPUT/OUTPUT CONTROLLER (IOC)
MEMORY DATA INTERFACE LOGIC
KEYWORD/ TERMINATION WORD INTERPRETATION AND UPDATE LOGIC
MEMORY ADDRESSING AND CONTROL LOGIC
FRONT PANEL AND MAINTENANCE
COMPUTER CONTROL PANEL LOGIC
CENTRAL PROCESSING UNIT
REAL-TIME CLOCK
INPUT/OUTPUT COMMAND INTERPRETATION LOGIC
PRIORITY/ ADDRESS DETERMINATION LOGIC
REAL-TIME CLOCK CALL-UP LOGIC
BYTE/WORD ASSEMBLY DISASSEMBLY LOGIC
INTERFACE CONTROLS GENERATION LOGIC
DEVICE REQUEST/ SELECT LOGIC
INPUT/OUTPUT BUS (DC)
1 TO 15 INPUT/OUTPUT EXCHANGERS
INPUT/ OUTPUT EXCHANGER IOX OR IOE
INPUT/ OUTPUT EXCHANGER IOX OR IOE
INPUT/OUTPUT UNIT (IOU)
INPUT/OUTPUT BUSES (AC) TO PERIPHERAL DEVICES
63-1-006

Figure 2-2. AN/GYK-12 Computer Input/Output Unit Functional Block Diagram

CHAPTER 3

AN/GYK-12 COMPUTER SPECIAL FEATURES

Section I. ADDRESSING

3-1. General

This section discusses the special features of the computer. The method of addressing memory in the computer is discussed along with the concept of the program level and related topics. The program activity register function and the program level auction function for controlling program level activity are explained. A discussion of the registers duplicated for each program level (multi-purpose process, indicator, instruction location, mask, trap, page control and address, privilege and level link, and queue registers) is presented. In addition, a discussion of the query, executive link and program registers (only one of each in the computer) is included.

3-2. Memory Addressing

The computer may have up to 16,384 memory pages of 2,048 thirty-two bit (plus parity) words each (total 33,554,432 words). However, only 16 of these pages may be physically active and addressable by a program level at any one time. Pages may be activated and deactivated under control of software by placing or overstoring the page address in one of the 16 page control and address registers for each of the 64 program levels.

a. *Page Control and Address Register.* A set of sixteen 16-bit half-words assigned to each of the 64 program levels are used to determine memory access control and memory page addressing. The page control and address registers are located in fixed memory locations as shown in figure F0-1. The page control and address registers for the active program level are changeable by instructions on that program level, only if the program level is privileged. The format of the page control and address register is shown in figure 3-1. There are two fields in the page control and address register.

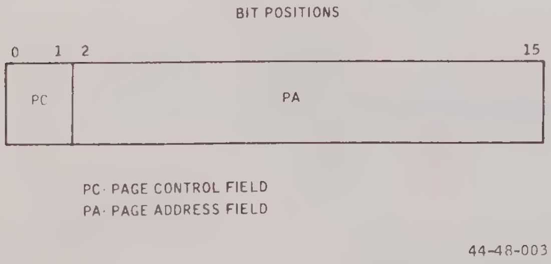


Figure 3-1. Page Control and Address Register Format

b. *PC, Page Control Field, Bit Positions 0 and 1.* Access to the memory page designated by the page address field is controlled by these two bits as shown in table 3-1. When an access violation occurs, the memory is not accessed, the appropriate bits in the indicator and query registers are set, and an automatic transfer to program level 2 is initiated.

c. *PA, Page Address Field, Bit Positions 2 to 15.* This field addresses the unique 2048 thirty-two bit word page of the 16,384 possible memory pages. The 14-bit page address field is appended to the 11-bit address field (A) of a memory reference to form the actual 25-bit memory address. The memory addresses 0000 to 003F$_{16}$ do not select a special address but always refer to the actual locations in memory whose real addresses are 0000 to 003F$_{16}$.

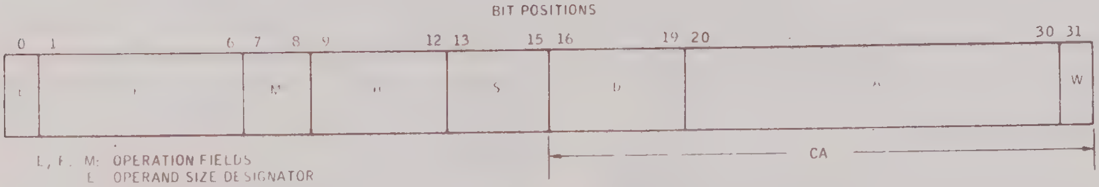
d. *Mechanism of Memory Addressing.* The operand address field (CA field) (figure 3-2) in the instruction word or any other memory reference address (figure 3-3) is 16 bits in length. Figure 3-2 illustrates the instruction word format and figure 3-3 illustrates the memory reference format. The CA field of the instruction word and the memory reference address format are both 16-bit addresses. The four most significant bits (D field) of the CA field and the memory reference address format, specify the page control and address register that is to be activated. The 11 bits that make up the A field specify the word to be selected. The one-bit W field specifies which half of the full word in memory will be selected. Figure 3-4 illustrates the more significant half of the full word in memory is selected if the W field equals zero. Figure 3-5 illustrates the less significant half of the full word in memory is selected if W equals one. Figure 3-6 illustrates the memory addressing mechanism. The data in this address performs 3 separate functions: it determines which page control and address register will be activated, the word to be selected on the memory page, and the half word of data that is to be extracted from the full word in memory at the address specified.

e. *PCA Register Addressing.* The PCA hardware registers can be addressed by any privileged program level. The effective instruction address should be (0020-002F)$_{16}$. The base memory locations associated with a given program level can be determined by taking the program level number in binary, shift it left 6 places, and add (002X)$_{16}$ to it. The X is (0-F)$_{16}$ depending on which PCA register is desired.

Table 3-1. Page Access Control Bits Operation

Page Access Control Bits	Name	Action Permitted			Action Inhibited		
00	Read-write access	Fetch instruction	Read operand	Write operand	-	-	-
01	Read access	Fetch instruction	Read operand	-	-	-	Write
10	Read Data access	-	Read operand	-	Fetch	-	Write
11	No access	-	-	-	Fetch	Read	Write

70061-2

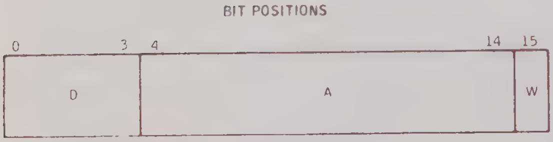

BIT POSITIONS
0
1
6
7
8
9
12
13
15
16
19
20
30
31
E
F
M
H
S
D
A
W
CA

E, F, M: OPERATION FIELDS
E: OPERAND SIZE DESIGNATOR
F: OPERATION CODE
I F: FUNCTION CODE
M: ADDRESS MODE SELECTOR
H: ACCUMULATOR DESIGNATOR
S: INDEX DESIGNATOR

CA OPERAND ADDRESS FIELD
D: PAGE DESIGNATOR
A: WORD ADDRESS DESIGNATOR
W: HALF WORD ADDRESS DESIGNATOR

63-1-007

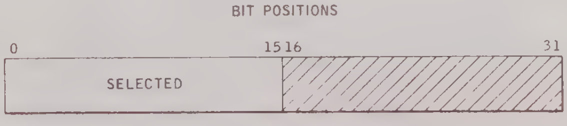
Figure 3-2. Instruction Word Format


BIT POSITIONS
0
3
4
14
15
D
A
W

D: PAGE CONTROL AND ADDRESS REGISTER DESIGNATOR (PAGE DESIGNATOR)
A: WORD ADDRESS DESIGNATOR
W: HALF WORD ADDRESS DESIGNATOR

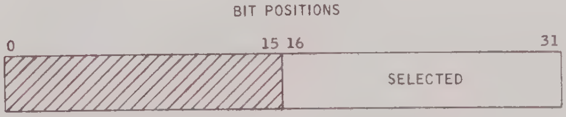
63-1-008

Figure 3-3. Memory Reference Address Format


BIT POSITIONS
0
15
16
31
SELECTED

44-48-005

Figure 3-4. Half Word Selected From Memory When W=0


BIT POSITIONS
0
15
16
31
SELECTED

44-48-006

Figure 3-5. Half Word Selected From Memory When W=1

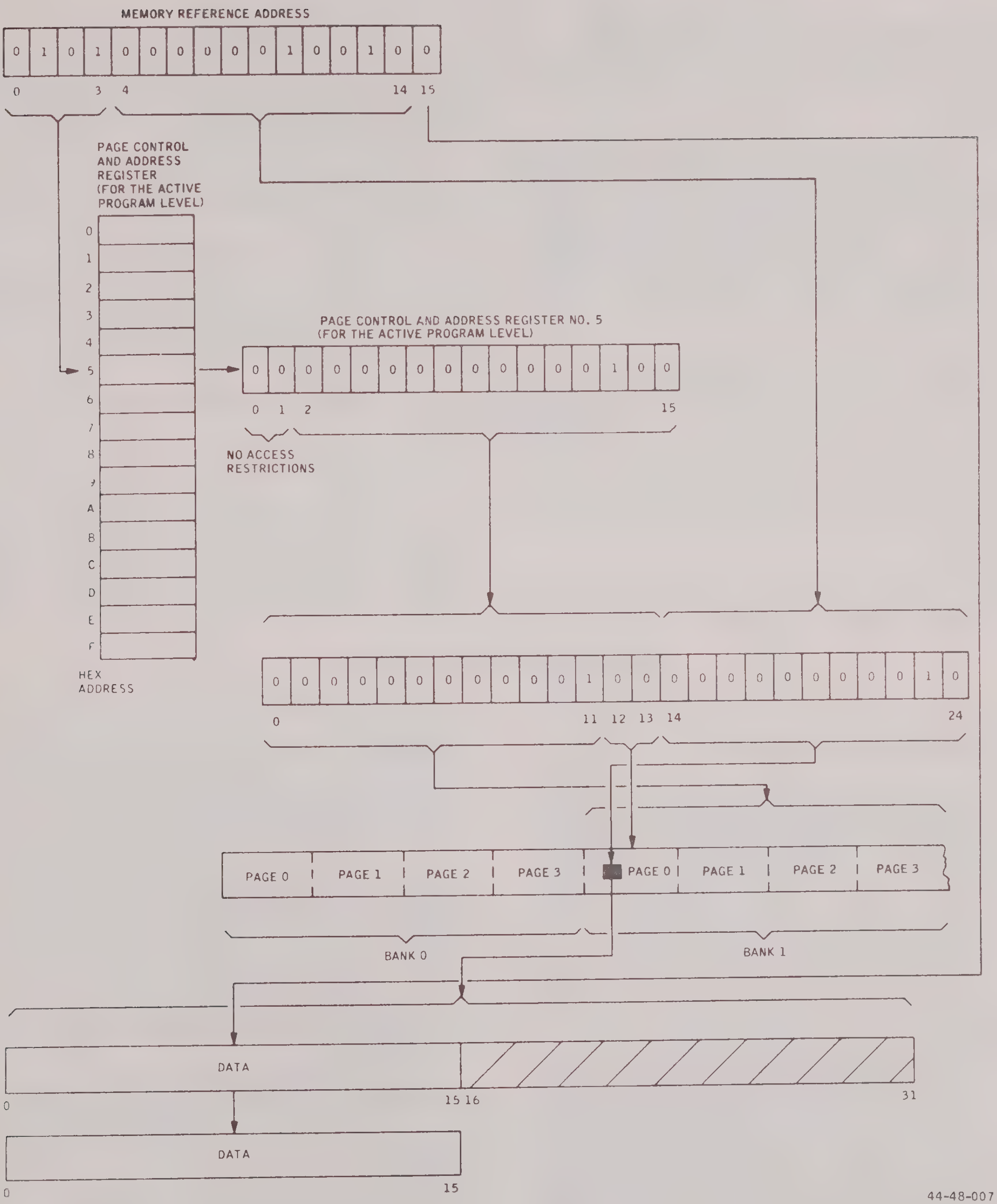

MEMORY REFERENCE ADDRESS
0 1 0 1 0 0 0 0 0 0 1 0 0 1 0 0
0 3 4 14 15
PAGE CONTROL AND ADDRESS REGISTER (FOR THE ACTIVE PROGRAM LEVEL)
0 1 2 3 4 5 6 7 8 9 A B C D E F
HEX ADDRESS
PAGE CONTROL AND ADDRESS REGISTER NO. 5 (FOR THE ACTIVE PROGRAM LEVEL)
0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0
0 1 2 15
NO ACCESS RESTRICTIONS
0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0 0 0 1 0
0 11 12 13 14 24
PAGE 0
PAGE 1
PAGE 2
PAGE 3
PAGE 0
PAGE 1
PAGE 2
PAGE 3
BANK 0
BANK 1
DATA
0 15 16 31
DATA
0 15
44-48-007

Figure 3-6. Mechanism of Memory Addressing

3-3. Memory Communication Characteristics

The computer provides for communication with multiple memory banks for information exchange and data exchange.

a. *Memory Interface.* The computer provides two to four independent memory interfaces with multiple memory banks. For a single central processing unit and input/output unit configuration, one memory interface is used for program controlled operations and another memory interface is used for automatic input/output operations. The memory interface includes control, address, and data lines.

b. *Data Exchange.* All data (instructions, indirect addresses, operands) is stored in or received from memory as 33 bit words, of which 32 bits represent data and one bit is an odd parity bit. The parity bit is such that the total number of one bits in the 33 bit word is an odd number. Correct parity is thus generated for all data words prior to storage in memory. Parity is examined for all data words received from memory. The detection of a memory parity error causes the following to occur:

(1) The operation is not performed.

(2) Memory is not changed.

(3) For program operations, bit position 9 of the active indicator register and bit position 0 of the query register are set. During program level changes, bit position 1 of the query register is set. The page designator which related to the detection of an error is set into positions 6 thru 9 of the query register.

Bit position 9 of indicator register is reset on next valid memory cycle. The query register bit positions are reset by software.

(4) For automatic input/output operations, bit position 11 or 12 of the monitor register and bit position 9 of the termination word are set. The addressed memory bank number is set into bit positions 21 thru 24 of the monitor register and the device address is set into bit positions 25 thru 31.

All of the above bit positions must be reset by software.

(5) A program level change to program level two is automatically initiated.

c. *Addressing.* A capability of addressing up to 33,554,432 words of 33 bits each is provided for program operations. The capability of addressing 131,072 words of 33 bits each is provided for automatic input/output operations. (See paragraph 4-8c for specific information.)

Section II. PROGRAM LEVELS

3-4. Definition of a Program Level

The computer is designed in such a manner that the hardware may control the activation and execution of up to 64 routines, one at a time on a priority demand basis. The computer hardware automatically administers a priority activation scheme and maintains the entry points for each of the 64 program levels (0-63_{10}) in a set of 64 instruction location registers. Each entry point is assigned a number on a priority scheme. This number is called a program level. There are 64 such program levels, with program level 63 the lowest priority, and program level 0 the highest priority. Each program level operates only if that program level is the highest priority active program level or if program control has been explicitly set to that program level. A program level may be designated active either by program action or by interrupts. The priority program level scheme allows entry points (levels) to be stacked and compete for activation. When a program level (entry point) is activated, the computer hardware retains the pertinent status information of the previously active program level, and begins execution of the new program level by executing the instruction at the address in the instruction location register for that program level. The control mechanism for the activation of the entry points which makes up the program levels is the status and enable bits in the program activity registers. Once an entry point has been activated, the hardware keeps track of its active state and the program level may be deactivated at any time. A program level is said to be active when both the corresponding status and enable bits of the program activity register are set to one and the entry point has been activated by the hardware. A program level may be inactive, waiting, stimulated, suspended, or operating as shown in table 3-2. A program level may also be interrupted. An interrupt occurs whenever a program level with a higher priority becomes activated by the hardware.

3-5. Mechanism of a Program Level Change Operation

Table 3-3 contains a program level change data summary. When a program level change is initiated, the computer performs one or a combination of the following actions, depending upon the initiation of program level change:

a. Detects conditions that cause a program level change.

b. Executes program level change by storing the process registers of the current program level in allocated memory addresses as specified in figure F0-1.

Table 3-2. Program Level Condition Due to Program Activity Register

Situation	PS Bit	PE Bit	Description
Inactive	0	0	Program level is disabled and idle
Waiting	0	1	Program level is enabled and is waiting for response from an external equipment or another program level.
Stimulated	1	0	Equipment responded or program level was stimulated but the program level has not been enabled.
Suspended	1	1	Program level suspended because program level of higher priority is currently being executed or program level lock has been set.
Operating	1	1	Program level is operating.

PS: Program level status bit
PE: Program level enable bit

70061-3

c. Load process registers, page control and address registers, and the privilege and level link register of the new program from the allocated memory address specified in figure F0-1 to the CPU's active registers.

d. Proceeds with program execution at the location taken from the instruction location register of the new program level.

e. Stores process registers, which are controlled by the program level change (LC) indicator bit for the call executive program level and link, call program level and link, tie program level and link, test and conditionally reset/skip, and device command and exit instructions. Loading of registers is controlled by the C-bits in the privilege and level link register of the new program level.

f. Stores and loads registers, which are controlled by C-bits in the privilege and level link register in the event of an interrupt.

g. Stores all process registers in the event of power turn off or error sequence.

h. A program level change will occur in a time period of from 20 to 150 microseconds depending upon how many registers are stored, how many registers are loaded, the memory speed, and memory interference by input/output.

3-6. Special Program Levels

Program levels 1 to 3 and 63 are reserved for the special functions discussed in the subsequent paragraphs.

a. *Level 1, Automatic Start Level.* When power is applied, the computer does not load the query register represented by special addresses 0034_{16} and 0035_{16} from the base memory bank, but resets the query register and enters and executes program level 1. Input/Output requests are serviced.

When an error has been detected in program level 1 then an automatic transfer to program level 2 is initiated.

NOTE

Detection of a system or power failure causes the storing of the program level register of the current program level in the base memory bank. The registers corresponding to special address 0034_{16} and 0035_{16} are stored in the base memory bank at those respective locations when not in program level 1 (power failure in program level 1 inhibits storing of the two special addresses). At the completion of the store operation, the CPU automatically halts. I/O requests are not serviced.

Instruction or Operation	Reset Level Lock	Set Level Lock	L1
TXP, Call Executive Program Level and Link		Yes	If (
TIE, Tie Program Level and Link		Yes	If (
TCP, Call Program Level and Link	Yes		If (
TQR, Test and Cond. Reset/Skip $Y < 40_{16}$ only	If (Y) = 0		If (
DEX, Device Command and Exit	Yes		Yes
LLO, Level Lock Set		Yes	
LLR, Level Lock Reset	Yes		
Power Off		Yes	
Error Exit (Enter Program Level 02)		Yes	
I/O Interrupt			
Power On		Yes	
Bootstrap Entry			

Table 3-3. Program Level Change Data Summary

T STB et tus	L2 SET STB Set Status Bit	L3 AUC PAR Auction of PAR Performed	L4 STR GRS Storing of Process Registers Based on	L5 FCN PLL Fetch Privilege and Control For New Level	L6 LOA PAG Loading of Page and Process Registers Based on	L7 STR QRR Store Query Register
Instruction						
	Yes	No, positive change to XPL	LC (CN01) Indicator	Yes	C field of XPL PLL register, unused pages unchanged	
	Yes	No, positive change to CPL	LC (CN01)	Yes	C field of CPI PLL register, unused pages unchanged	
	Yes	Yes	LC (CN01)	Yes	C field of PLL registers for new level, unused pages inaccessible	
= 0		Yes	LC (CN01)	Yes	C field of PLL registers for new level, unused pages inaccessible	
		Yes	LC (CN01)	Yes	C field of PLL registers for new level, unused pages, inaccessible	
Operation						
			All process registers are stored	No	Loading not performed	Yes No, when in Program Level 01
	Yes, for Program Level 02	No, positive change to Program Level 02	All process registers are stored	Yes, for Program Level 02	C field of PLL registers for Program Level 02, unused pages inaccessible	
	Set by IOC	Yes	C (bit 08) of PLL register for previous level	Yes	C field of PLL registers for new level, unused pages inaccessible	
				No, PV = 10	All registers loaded	
				No, PV = 10	All registers loaded	

70061-4

b. *Level 2, Error Level.* Program level two (02), is often called 'Error Level'; it should be distinguished from the EPL (Error Program Level) specified by termination of input/output operations.

Program level 2 is automatically entered under a number of hardware conditions. Every condition which causes a change to program level 2 also posts a bit in either the query register or the monitor register. The query register is associated with the instruction controller, while the monitor register is associated with error detection logic within the IOC. When program level 2 is entered, all peripheral device requests are honored by the IOC, including the three real time clocks.

The program level lock is automatically set when a hardware initiated transfer to program level 2 occurs and the status bit is also set. (The enable bits for program level 1, 2, and 3 in the program activity register should be set to a ONE.)

Once a transfer to program level 2 has been initiated due to an error condition, all further error conditions will be detected. However, a second error condition which has been detected either by the instruction controller or input output controller (IOC) will set the Error Exit (EE) bit in the query register. When the EE bit has been set, then an attempt to leave program level 2 will return the program to program level 2.

All error conditions which result in a hardware initiated transfer to program level 2 are as follows:

(1) Instruction controller detected errors (query register).

(a) IPE, Instruction Parity Error, Bit Position 0. This bit is set when a memory parity error is detected during instruction execution. The detection occurs during instruction access, indirect address access, and operand access. The instruction experiencing the parity error is not executed.

(b) LPE, Level Change Parity Error, Bit Position 1. This bit is set when a memory parity error is detected during the course of exchanging program level registers in a program level change.

(c) IV, Instruction Violation, Bit Position 2. This bit is set when an instruction privilege violation, or a special address privilege violation is detected during program execution.

(d) MV, Memory Access Violation, Bit Position 3. This bit is set when memory access violation is detected during program execution.

(e) MTO, Memory Time-Out, Bit Position 4. This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request during program execution.

(f) SV, Specification Violation, Bit Position 5. This bit is set when an instruction is detected for which mode 0 is excluded, or when the address refers to an excluded special address.

(g) D, Page Designator, Bit Positions 6 to 9. This four-bit field designates the page control and address register which is related to the detection of a memory parity error, access violation, or no response time out. When any bit, 0-5 is set, the D field is inhibited from being changed by any subsequent error condition.

(h) PPL, Prior Program Level, Bit Positions 10 to 15. This six-bit field indicates the program level that experienced an error condition or the prior active program level. This field is not changed when entering the trace program level. When start-up occurs after power shutdown, this field contains the program level number in which power shutdown occurs.

(i) EE, Error Exit, Bit Position 17. This bit will be set and reset by hardware only; it can be read by software, but it cannot be changed (set or reset) by software.

When the EE bit is ZERO and a program in program level 2 attempts an exit, it will exit.

This bit is set whenever a program is in program level 2 and an error is detected by either the CPU or IOC which would have resulted in a program level 2 entry. An attempt to exit program level 2 while the EE bit is set, will result in a return to program level 2; at the same time, the EE bit will be reset.

When any bit positions 0 to 5 in the query register is a ONE, and the instruction controller detects an error, then bit positions 0 to 15 will not be changed, but the EE bit will be set.

(j) APL, Active Program Level, Bit Positions 26 to 31. This six bit field indicates the currently active program level.

(2) Instruction controller detected errors (indicator register). When an error is detected during program execution, then a bit is set in the indicator register and the query register.

(a) PV, Privilege Violation, Bit Position 7. This bit is set by a privileged instruction violation, special address violation, memory access violation, mode 0 excluded violation, or an excluded special address violation.

(b) ME, Memory Parity Error, Bit Position 9. This bit is set whenever a memory parity error is detected during a non I/O and non-program-level change operation. This may occur on a memory read operation or on a memory store operation when the quantity to be stored is less than 32 bits and the remaining bits are to remain unchanged.

(3) Input output controller (IOC) detected errors (monitor register).

(a) Input on Output Error, Bit Position 7. This bit is set when a peripheral device inputs data while the keyword specifies output modes 1, 4 or 5.

(b) Device Time Out, Bit Position 9. This bit is set when a peripheral device time out occurs during an I/O operation (peripheral device hangup). This bit is set when a peripheral device is not responding to the IOCs address/enable sequence within 10 microseconds in the automatic input mode.

(c) I/O Memory Access Violation, Bit Position 10. This bit is set when a memory access violation occurs during an input or output operation.

(d) I/O Memory Parity Error on Control Word, Bit Position 11. This bit is set when the IOC detects a memory parity error when accessing the base memory bank (keyword, termination word, program activity register, queue register).

(e) I/O Memory Parity Error on Data Word, Bit Position 12. This bit is set when the IOC detects a memory parity error when accessing memory for data transfers (full word output, byte output, byte input).

(f) Memory Time Out Bit Position 13. This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request by the IOC.

(g) IOC Time Out, Bit Position 14. This bit is set when the IOC fails to honor a real-time clock request (any of the three) within 256 microseconds (2048 microseconds in NICS-TARE).

(h) Program Time Out, Bit Position 15. This bit is set when the IOC detects that the keyword block length field for the real time clock "zero" (peripheral device address 03) is zero. The program should have reinitialized this field within 1,024 microseconds (8,192 microseconds in NICS-TARE) after it has been decremented to zero.

(i) I/O Avalanche Error, Bit Position 16. (Not used in AN/TSQ-73.) The setting of any bit positions 7, 9 through 15 indicates that an error has occurred which stimulated program level 2. The setting of any one of these bit positions will set a flip-flop (not related to bit position 16) inhibiting any further setting until an OFR instruction to peripheral device address 01 or 02 has been executed. This OFR instruction will enable the setting of bit positions 7, 9 through 15 in the monitor register; the OFR instruction is effective even when all bits in the selected process register are all zeros.

The avalanche error, bit position 16, will be set when the IOC detects a second I/O related error before a first error (which stimulated program level 2) has been cleared by executing an OFR instruction to peripheral address 01 or 02.

(j) Memory Bank Address, Bit Positions 21 through 24. Bit position 21 is ZERO, bit position 22 is the most significant bit of the memory address. These bits are set when the IOC detects one of the following conditions:

1. Memory parity error.
2. Memory access violation.
3. Memory time out.

(k) Device Address, Bit Positions 25 through 31. Bit position 25 is ZERO, bit position 26 is the most significant bit of the peripheral device address. These bits are set when the IOC detects an error which causes to set any bit positions 7, 9 through 15.

NOTE

The device address bits are also set under two conditions which do not stimulate program level 2. First, when an input parity error is detected during bootstrap program load, monitor register bit 8 will be set and the IOC stops. Second, when an input parity error is detected during an automatic input and the P-bit in the termination word is a ONE. The program level (EPL) as specified in the termination word will be stimulated (not program level 2, unless EPL = 2); the device address may be ambiguous for this second case.

c. *Level 3, Trace Level.* Program level 3 is entered automatically and temporarily when a program level change is attempted and the switch on the computer test set (CTS) or System Control Console (SCC) is in the ON position. The query register contains the tentative program level which represents the destination program level. An exit from this program level does not change the prior program level field in the query register. When program level 03 is entered with the LEVEL TRACE switch ON, the PCA and Process registers are loaded under control of the 'C' bits of the TENTATIVE Program Level in the Privilege and Level Link Word (see paragraph 3.15c). Therefore, caution should be used when programming in program level 03.

d. *Level 63, Bootstrap Program Load Level.* Program level 63 is entered after execution of a bootstrap program load.

3-7. Changing Program Levels

There are three basic reasons for program level changes to occur in the computer: a machine instruction is executed which causes a program level change to take place; an internal or external fault occurs, and an I/O operation comes to a conclusion.

a. *Program Level Changes Caused by Instruction Execution.* Program level changes can be programmed by machine instruction. Two instructions (TXP and TIE) call for program level changes and specify the program level to which the change is to take place. Three instructions (TCP, TQR and DEX) call for program level changes and create an 'auction'. An 'auction' means that, rather than go to a directly specified program level, a scan of the program activity register (PAR) takes place. The program level that will be activated by the scan of the PAR is the highest priority program level with program status and program enable bits both set to one.

b. *Program Level Changes Caused by Fault Detection.* A program level change caused by the detection of a fault is an interrupt. Interrupts can be caused by software mistakes (programming mistakes) or by errors detected in the hardware. Almost all of these detected mistakes and errors result in an automatic program level change to program level 2. These include memory access violations (CPU/IOU), privilege violations (CPU), operational errors (IOU), memory parity error (CPU/IOU), device time outs (IOU), real-time clock time outs (IOU), memory time outs (CPU/IOU) and specification violations (CPU).

c. *Program Level Changes Resulting From the Conclusion of I/O Operations.* The conclusion of an I/O operation always causes an interrupt whether the operation was successful or unsuccessful. A successful I/O operation interrupts the current program operation with a transfer to the normal program level (NPL) which is designated prior to the initiation of the I/O operation if NPL is of higher priority than the Active Program Level (APL). The unsuccessful conclusion of an I/O operation can cause an interrupt to program level 2 or to an error program level (EPL). The EPL is designated prior to the initiation of the I/O operation. It should be noted that if the C-Control bit in the termination word is set to one, then the IOU initiates the program level change (channel interrupt). Otherwise, the peripheral device must perform the interrupt (device interrupt).

NOTE

If the program level lock is set, all nonprogram level 2 interrupts are posted and processed when the program level lock is reset. Program level 2 interrupts will occur regardless of the setting of the program level lock. Power off will cause a locked-in program level to be interrupted.

Section III. SPECIAL PURPOSE REGISTERS

3-8. General

There are a number of special purpose registers in the computer. These registers are located in memory in permanently assigned locations as shown in figure F0-1. Some of them are common to all program levels and there is only one of each in the computer. Others are duplicated for each program level.

3-9. Common Registers

There is one of each of the following special registers in the computer:

a. Query register – $(0034\text{-}35)_{16}$

b. Executive link register – $(0036\text{-}37)_{16}$

c. Program activity register – $(0038\text{-}3F)_{16}$

3-10. Query Register

The query register contains information pertaining to recognized error conditions in program execution and stipulates the currently active program level. The query register is common to all program levels and is assigned base memory bank addresses 0034_{16} and 0035_{16}. Access to the query register is reserved for privileged programs. It is stored on power shutdown. The query register is not stored when power shutdown occurs in program level 1. Power-on master resets the query register (base memory bank is not reset). The word format is as shown in figure 3-7.

a. *IPE, Instruction Parity Error, Bit Position 0.* This bit is set when a memory parity error is detected during instruction execution. The detection occurs during instruction access, indirect address access, and operand access. The instruction experiencing the parity error is not executed.

b. *LPE, Level Change Parity Error, Bit Position 1.* This bit is set when a memory parity error is detected during the course of exchanging program level registers in a program level change.

c. *IV, Instruction Violation, Bit Position 2.* This bit is set when an instruction privilege violation, or a special address privilege violation occurs during program execution.

d. *MV, Memory Access Violation, Bit Position 3.* This bit is set when memory access violation occurs during program execution.

e. *MTO, Memory Time-Out, Bit Position 4.* This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request during program execution.

f. *SV, Specification Violation, Bit Position 5.* This bit is set when an instruction is detected for which mode 0 is excluded, or when the address refers to an excluded special address. This bit is also set when a secondary CPU (without an IOU) attempts the execution of an input/output instruction.

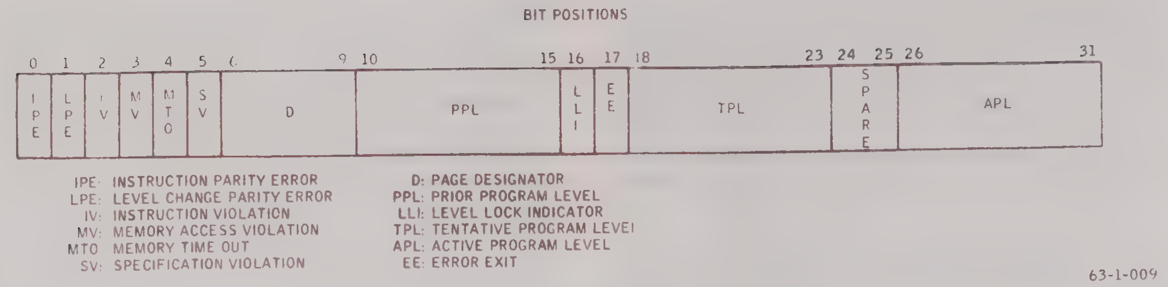

BIT POSITIONS
0
1
2
3
4
5
6
9
10
15
16
17
18
23
24
25
26
31
IPE
LPE
IV
MV
MTO
SV
D
PPL
LLI
EE
TPL
SPARE
APL
IPE: INSTRUCTION PARITY ERROR
LPE: LEVEL CHANGE PARITY ERROR
IV: INSTRUCTION VIOLATION
MV: MEMORY ACCESS VIOLATION
MTO MEMORY TIME OUT
SV: SPECIFICATION VIOLATION
D: PAGE DESIGNATOR
PPL: PRIOR PROGRAM LEVEL
LLI: LEVEL LOCK INDICATOR
TPL: TENTATIVE PROGRAM LEVEL
APL: ACTIVE PROGRAM LEVEL
EE: ERROR EXIT
63-1-009

Figure 3-7. Query Register Format

g. *D, Page Designator, Bit Positions 6 to 9.* This four-bit field designates the page control and address register which is related to the detection of a memory parity error, access violation, instruction violation, specification violation, or no response time out. When any bit, 0-5 is set, the D field is inhibited from being changed by any subsequent error condition.

h. *PPL, Prior Program Level, Bit Positions 10 to 15.* This six-bit field indicates the program level that experienced an error condition or the prior active program level. This field is not changed when entering the trace program level. When startup occurs after power shutdown, this field contains the level number in which power shutdown occurs. Note, in this case base memory must be accessed.

i. *LLI, Level Lock Indicator, Bit Position 16.* This bit is set with the level lock set, call executive program level and link, or tie program level and link instruction. This bit is reset with the level lock reset, or call program level and link, or device command and exit instruction, and conditionally reset with the test and conditionally reset/skip. The level lock indicator is not set by error conditions, power on, power off, or bootstrap program load.

j. *EE, Error Exit, Bit Position 17.* This bit will be set and reset by hardware only; it can be read by software, but it cannot be changed (set or reset) by software.

When the EE bit is ZERO and a program in program level 2 attempts an exit, it will exit.

This bit is set whenever a program is in program level 2 and an error is detected by either the CPU or IOC which would have resulted in a program level 2 entry. An attempt to exit program level 2 while the EE bit is set, will result in a return to program level 2; at the same time, the EE bit will be reset.

When any bit positions 0 to 5 in the query register is a ONE, and the instruction controller detects an error, then bit positions 0 to 15 will not be changed, but the EE bit will be set.

k. *TPL, Tentative Program Level, Bit Positions 18 to 23.* This six-bit field indicates the program level which represents the destination program level when the trace program level is entered. During startup, TPL $= 63_{10}$.

l. *Spare, Bit Positions 24 and 25.*

m. *APL, Active Program Level, Bit Positions 26 to 31.* This six-bit field indicates the currently active program level.

3-11. Executive Link Register

The executive link register contains information pertinent to program linkage with the executive program level. This register is common to all program levels and assigned base memory bank address 0036_{16}. The executive link register is used by the call executive program level and link instruction (TXP). Program access to the addressable executive link register requires a privileged status. The word format is as shown in figure 3-8. The six-bit field XPL specifies the executive program level to which a transfer is called for by a call executive program level and link instruction.

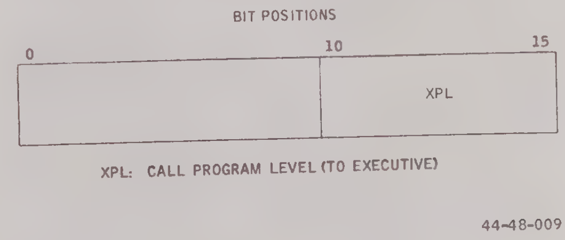

BIT POSITIONS
0
10
15
XPL
XPL: CALL PROGRAM LEVEL (TO EXECUTIVE)
44-48-009

Figure 3-8. Executive Link Work Format

3-12. Program Activity Register

The control and status of program levels are maintained by the program activity register (PAR) which is addressable. This register contains 128 bits, consisting of eight 16-bit half words. Four half words represent the program level status (PS), and four half words represent the program level enable (PE). The contents of a pair of status-enable bits determine the operating condition for a program level as indicated in table 3-2.

set by interrupt

0034

LOCATION	PROGRAM LEVEL STATUS BITS	PROGRAM LEVEL ENABLE BITS
0038_{16}	0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
$003A_{16}$	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31	16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
$003C_{16}$	32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47	32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47
$003E_{16}$	48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63	48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
	HALF-WORD 0	HALF-WORD 1

NOTE:
PROGRAM LEVEL 0 IS HIGHEST PRIORITY
PROGRAM LEVEL 63 IS LOWEST PRIORITY

A44-48-010

Figure 3-9. Program Activity Register Format

The bit position in the PAR is as specified in figure 3-9. The lower the program level number, the higher the priority. Status bits and enable bits are set or reset by the execution of computer instructions in privileged program levels only. Status bits are also set as a result of any one of the following conditions:

a. Terminated input/output operation.

b. Call program level and link instruction.

c. Call executive program level and link instruction.

d. Tie program level and link instruction.

e. Power on (program level one).

f. Error condition (program level two).

g. Trace (program level three).

Status bits are also reset by the device command and exit instruction and conditionally reset by any one of the following instructions:

a. Call program level and link.

b. Call executive program level and link.

c. Tie program level and link.

d. Test and conditionally reset/skip.

3-13. Program Level Associated Registers

There is one or one set of each of the following special registers for each program level.

a. 16 process registers.

b. 16 Page Control and Address (PCA) registers (see para 3-2a).

c. Privilege and level link register.

d. Queue register.

3-14. Process Registers

A set of sixteen 32-bit words are assigned to each of the 64 program levels and are used for index registers, accumulators, and special control. The process registers for the active program level are addressed using the special addresses 00-1F$_{16}$. Table 3-4 represents the address configuration and designators for the active process registers. The following process registers are reserved for special functions.

- Indicator register.
- Instruction location register.
- Mask register.
- Trap register.

a. *Indicator Register.* The 16 most significant bits of process register 0 (half-word address 0) contain the indicators and flags for the program level. Figure 3-10 represents the indicator register format with the functions defined in the subsequent paragraphs.

Table 3-4. Use of the 16 Process Registers (32 Bits Each)

Half-Word Address (Hexadecimal)	H (Decimal)	S	Number of Bits	Function
0	0		16	Indicator register
1	0		16	Instruction location register
3		1	16	
5		2	16	
7		3	16	
9		4	16	Index registers
B		5	16	
D		6	16	
F		7	16	
0, 1	0		32	(Do not use)
2, 3	1		32	
4, 5	2		32	
6, 7	3		32	
8, 9	4		32	
A, B	5		32	
C, D	6		32	
E, F	7		32	Accumulators
10, 11	8		32	
12, 13	9		32	
14, 15	10		32	
16, 17	11		32	
18, 19	12		32	
1A, 1B	13		32	
1C, 1D	14		32	Mask register
1E, 1F	15		32	Trap instruction

70061-5

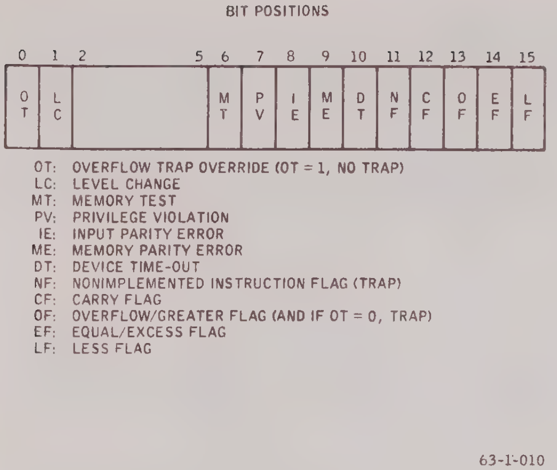


Figure 3-10. Indicator Register Format

(1) *OT, Overflow Trap Override, Bit Position 0.* If this bit is a ZERO and a fixed-point arithmetic overflow occurs, the instruction traps by excuting the instruction which has been previously stored in process register 15 (normally a transfer and link instruction). If this bit is a ONE, trap on overflow does not occur.

(2) *LC, Level Change, Bit Position 1.* This bit is set by hardware when a program level is being entered.

When this bit is a ONE during the execution of a call executive program level and link, or call program level and link, or tie program level and link, or test and conditionally reset/skip (conditionally), or device command and exit instruction then process register 0 only is saved during the program level change.

When a program resets the LC bit prior to the execution of one of the above listed instructions, then all process registers are saved. When an interrupt (program level change) occurs between the resetting of the LC bit and the execution of one of the above listed instructions, then the LC bit is set by reentering the program level after the interrupt.

A program level change caused by an interrupt (other than the above listed instructions) will use the C bit in the privilege and link word for storing the process registers.

(3) *MT, Memory Test, Bit Position 6.* This bit is set when the acceptance line on the memory communication network is not activated by the memory bank, indicating an error during a memory bank assignment or test operation.

(4) *PV, Privilege Violation, Bit Position 7.* This bit is set by a privileged instruction violation, special address privilege violation, memory access violation, mode 0 excluded violation, or an excluded special address violation. An automatic transfer to program level 2 is also initiated.

(5) *IE, Input Parity Error, Bit Position 8.* This indicator bit is reset at the start of each input to register instruction. This bit is set when a parity error on the I/O communication network is detected during the execution of an input-to-register instruction. (Program level 2 is not activated.)

(6) *ME, Memory Parity Error, Bit Position 9.* This bit is set whenever a memory parity error is detected during a non-I/O and non-program-level change operation. This may occur on a memory read operation or on a memory store operation when the quantity to be stored is less than 32 bits and the remaining bits are to remain unchanged. An automatic transfer to program level 2 is also initiated.

This bit is reset on the next valid memory cycle after entering the program level.

(7) *DT, Device Timeout, Bit Position 10.* This bit is reset each time an I/O instruction is executed. It is set if the indicator signal on the I/O communication network is not detected within the allotted 10-microsecond response period. (Program level 2 not affected, monitor register, bit 9, not affected, program level 2 not activated.)

(8) *NF, Nonimplemented Instruction Flag, Bit Position 11.* This bit is set when a nonimplemented instruction code is detected. The instruction traps by executing the instruction located in process register 15.

(9) *CF, Carry Flag, Bit Position 12.* This bit is reset at the start of an arithmetic instruction and is set if there is a carryover from the most significant bit (sign) position in an arithmetic operation.

(10) *OF, Overflow/Greater Flag, Bit Position 13.* This bit is reset at the start of arithmetic and compare instructions. It is set when the final result is not within the numerical range of a word. An overflow flag is not set when a temporary overflow occurs. If the OT bit is a ZERO, a trap is initiated. This bit is set when a compare instruction finds a greater condition and no trap occurs.

(11) *EF, Equal/Excess Flag, Bit Position 14.* This bit is reset at the start of compare instructions and is set when the instruction finds an equal condition. This bit is also set as specified by the individual instruction, when a numerical value exceeds 16 bits (bit positions 0 thru 16 are not all ZEROS or not all ONES).

(12) *LF, Less Flag, Bit Position 15.* This bit is reset at the start of compare instructions and is set when the instruction finds a less condition.

b. *Instruction Location Register.* The 16 least significant bits of process register 0 (half word address 1) contains the address of the next instruction in sequence (except when modified by the current instruction) for the program level. Figure 3-11 represents the instruction location register format with the functions defined as follows:

(1) *D, Page, Bit Positions 16 to 19.* These four bits select one of the 16-page control and address registers associated with the program level. Page designation does not apply whenever a special address is encountered.

(2) *A, Word Address, Bit Positions 20 to 30.* These eleven bits select one of 2048 words in a page.

(3) *W, Half-Word Address, Bit Position 31.* This bit is ignored. It is always ZERO.

c. *Mask Register.* Process register 14 is the register which contains the information to be used in an instruction requiring a mask.

d. *Trap Register.* Process register 15 is the register which contains the instruction to be executed when a trap condition occurs. The trap condition occurs on an attempt to execute a nonimplemented instruction. It also occurs on an arithmetic overflow when the overflow trap override bit of the indicator register is equal to zero.

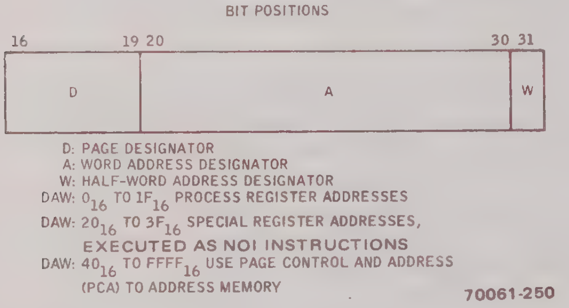

BIT POSITIONS
16
19 20
30 31
D
A
W
D: PAGE DESIGNATOR
A: WORD ADDRESS DESIGNATOR
W: HALF-WORD ADDRESS DESIGNATOR
DAW: 0_{16} TO $1F_{16}$ PROCESS REGISTER ADDRESSES
DAW: 20_{16} TO $3F_{16}$ SPECIAL REGISTER ADDRESSES, EXECUTED AS NOI INSTRUCTIONS
DAW: 40_{16} TO $FFFF_{16}$ USE PAGE CONTROL AND ADDRESS (PCA) TO ADDRESS MEMORY
70061-250

Figure 3-11. Instruction Location Register Format

3-15. Privilege and Level Link Register

Each of the 64 program levels has been assigned a control register which contains program level link information and privilege status. These control registers are allocated to the base memory bank half-word addresses 0030_{16} and 0031_{16} of each program level.

Direct program modification of these addressable control words require a privileged status. The privilege and level link word is required specifically in the execution of the call program level and link, call executive program level and link, and tie program level and link instructions. The word format shown in figure 3-12 is defined in the subsequent paragraphs.

a. *P, Privilege Status, Bit Positions 0 and 1.* Table 3-5 shows the assignment of these two bits.

These bits when equal to ZERO-ZERO, indicate that the associated program level is permitted to execute only non-privileged instructions; (excluded are privileged instructions, semi-privileged instructions, and access to restricted special addresses).

These bits, when equal to ZERO-ONE, indicate that the associated program level is permitted to execute semi-privileged instructions (see chapter 6) and non-privileged instructions.

These bits, when equal to ONE-ZERO, indicate that the associated program level is permitted to execute all instructions, privileged, semi-privileged, non-privileged, and access all registers represented by a special address.

b. *LPL, Link Program Level (From) Bit Positions 2 to 7.* This 6-bit field contains the program level number of the previous program level that was executed prior to the program level change. Call program executive level and link, call program level and link, or a tie program level and link instruction causes the LPL field to be modified.

c. *C, Level Control, Bit Positions 8 and 9.* When a program level change takes place in response to a non-software initiated interrupt, then these two bits control the storing and loading of registers as specified in table 3-6.

When a program level change takes place in response to a software instruction, then two bits control the loading of registers of the new program level as specified in table 3-7. The software instructions affecting this program level change are listed in table 3-7. The storing of the process registers, associated with the old program level which executes an instruction listed in table 3-7, are under control of the LC-bit in the indicator register.

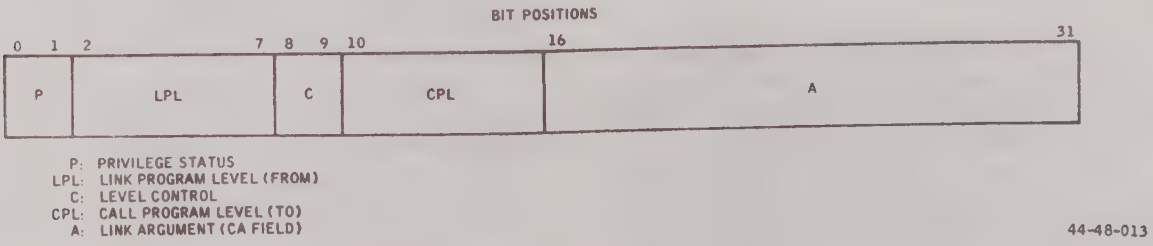

BIT POSITIONS
0
1
2
7
8
9
10
16
31
P
LPL
C
CPL
A
P: PRIVILEGE STATUS
LPL: LINK PROGRAM LEVEL (FROM)
C: LEVEL CONTROL
CPL: CALL PROGRAM LEVEL (TO)
A: LINK ARGUMENT (CA FIELD)
44-48-013

Figure 3-12. Privilege and Level Link Word Format

Table 3-5. P Field Program Level Privileged Status

P Field		Program Level Privileged Status
Bit Position 0	Bit Position 1	
0	0	Non privileged
0	1	Semi-privileged
1	0	Privileged
1	1	Not assigned

70061-6

Table 3-6. Storing and Loading of Registers Due to Non-Software Initiated Interrupts

C Field		Storing Due to Non-Software Initiated Interrupts	Loading of New Program Level Registers Due to Non-Software Initiated Interrupts
Bit Position 8	Bit Position 9		
0	0	Store all process registers.	Load all process and page control and address registers for the new program level.
0	1	Store all process registers.	Load all process registers. Load page control and address registers 0-3. Page control and address registers 4-15 remain unchanged. Reference to page control and address registers 4-15 as the effective D field of an instruction or operand fetch will result in an Access Violation.
1	0	Store process register 0 only.	Load process register 0 only. Load all page control and address registers.
1	1	Store process register 0 only.	Load process register 0 only. Load page control and address registers 0-3. Page control and address registers 4-15 remain unchanged. Reference to page control and address registers 4-15 as the effective D field of an instruction operand memory fetch will result in an Access Violation.
		Note. Storing is affected by bit positions 8 and 9 in the old program level's privilege and level link word.	Note: Loading is affected by bit positions 8 and 9 in the new program level's privilege and level link word.

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Table 3-7. Storing and Loading of Registers Due to Software Instructions

Instructions:

TXP	Call Executive Program Level and Link
TCP	Call Program Level and Link
TIE	Tie Program Level and Link
TQR	Test and Conditionally Reset/Skip*
DEX	Device Command and Exit

*Only when TQR instruction initiates a program level change

Storing of Process Registers due to Software Initiated Program Level Changes

The LC bit in the indicator register determines the storing of process registers for the current program level.

If LC = 0 store all process registers of the current program level.

If LC = 1 store process register 0 of the current program level.

C Field		Loading of Registers Due to Software Initiated Program Level Changes
Bit Position 8	Bit Position 9	
0	0	Load all process registers and page control and address registers.
0	1	Load all process registers and page control and address registers 0 to 3. Page control and address registers 4 to 15 are left unchanged. Reference to page control and address registers 4-15 as the effective D field of an instruction or operand memory fetch will result in an Access Violation.
1	0	Load process register 0 and all page control and address registers.
1	1	Load process register 0 and page control and address registers 0 to 3. Page control and address registers 4 to 15 are left unchanged. Reference to page control and address registers 4-15 as the effective D field of an instruction or operand memory fetch will result in an Access Violation.

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d. *CPL, Call Program Level (To), Bit Positions 10 to 15.* This six-bit field specifies the program level to which a transfer is called for by a call program level and link or tie program level and link instruction.

e. *A, Link Argument, Bit Positions 16 to 31.* Information is communicated to a called program from the calling program by use of this 16-bit field. The half-word operand addressed in a call program level and link call executive program level and link or tie program level and link instruction is placed in the link argument field of the called program level's privilege and level link word.

(1) For call and tie instructions, bit 16 of the operand is tested, and if equal to ZERO, the status bit corresponding to the operating program level is reset.

(2) For the call program level and link instruction, bit 17 is checked and if equal to one, program level 63 is stimulated.

(3) For the call program level and link instruction, bit 18 is checked and if equal to one, a bit is set in the queue register of the called program level. The bit position to be set in the queue register is specified by bit positions 19 through 23 of the A field.

3-16. Queue Register

Each of the 64 program levels has an assigned control register which contains 32 bits used in program level communications. A bit position in this register is set as specified in the call program level and link instruction. A bit position is also set as specified in the termination word. A bit position is reset as specified in the test and conditionally reset/skip instruction when address 32_{16} is specified.

3-17. Cause and Effect of Error Conditions and Interrupts

Table 3-8 lists the error conditions and interrupts that can be encountered during program execution. Also listed in the table is the cause of the condition (software or hardware) and the effect the condition has upon the continuation of program execution.

Table 3-8. Cause and Effect of Error Conditions and Interrupts

Name of Violation, Interrupt or Error Condition	Software Caused	Hardware Caused	Program Level 2 (Error)	Normal Program Level Exit	Error Program Level Exit	Trap to Process Register 15	Results in a No Operation
Memory Parity		X	X				
Instruction Violation Privilege Violation	X		X				
Memory Access Violation	X	X	X				
Memory Time-Out	X	X	X				
Specification Violation	X		X				
Overflow	X					X[2]	
Divide Fault	X					X[2]	X
Replace Square Root Fault	X					X[2]	X
Non-Implemented Instruction	X					X	
Device Time-Out (IOU)	X	X	X				
Device Time-Out (CPU)	X	X					
IOC Time-Out (Any Real Time Clock)	X	X	X				
Program Time-Out (Real Time Clock 0)	X		X				
I/O Termination (successful)		X		X			
I/O Termination (unsuccessful)		X	X[1]		X[1]		

[1] Most I/O errors are program level 2 errors (see Chapter 4).

[2] Trap only occurs if the OT indicator is set to zero.

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CHAPTER 4

AN/GYK-12 COMPUTER INPUT/OUTPUT CHARACTERISTICS

Section I. INTRODUCTION

4-1. General

This chapter presents detailed information pertaining to the input/output (I/O) characteristics of the computer. Methods employed by the computer to control the execution of data communication with peripheral devices are discussed. A simplified block diagram showing the interface between the computer and the peripheral devices is presented. The programmed I/O communication class, automatic I/O communication class, modes of operation, types of operation, I/O memory access control, real-time clocks, typical peripheral device operation, diagnose feature, and front panel and maintenance are also discussed. Two classes of operation are used to enable the computer to provide control for the execution of data communication with peripheral devices. The two classes of operations are:

a. The programmed input/output (I/O) communication class.

b. The automatic input/output (I/O) communications class.

Programmed I/O communications are provided by four computer instructions (discussed in paragraph 4-4). Automatic I/O communications are independent of instruction execution, take place at the peripheral device rate, and are controlled by special I/O control words. The control words are the keyword and the termination word (discussed in paragraph 4-5). Automatic I/O communications are initiated by programmed instructions.

NOTE

All references herein to input is input to the computer and reference to output is output from the computer.

4-2. Input/Output Unit (IOU)

The input/output unit (IOU), independent of the CPU, largely controls communication between the memory and the peripheral devices. The IOU is comprised of the following items:

a. Input/output controller (IOC).

b. Front panel and maintenance.

c. Input/output exchangers (IOX/IOE).

d. Real-time clock.

4-3. Schematic Arrangement

Figure 4-1 is a simplified block diagram showing the external interface between the computer and the peripheral devices via the input/output controller (IOC) over its input/output data exchange (IOX) communication channel. From one to 15 IOX's or IOE's may be connected to the computer, at one time, to provide a total of up to 15 communication channels; each capable of handling eight peripheral devices. Thus 120 peripheral devices plus the internal real-time clocks and computer front panel can be accommodated. The peripheral device address selection and peripheral device priority are discussed in the subsequent paragraphs.

a. *Peripheral Device Address Selection.* Each peripheral device has an optional device address select switch which permits the selection of one of the eight subaddresses. The device address of the peripheral device is determined by the switch setting and upon the communication channel to which it is connected. The device address is a two-digit-octal number; the most significant digit represents the communication channel numbers and the least significant digit represents the device address switch setting. For example, when the switch in a peripheral device is set to position 3 and the device is connected to an IOX which is set to position 6, the device address will be 63 (octal).

b. *Peripheral Device Priority.* The servicing of the peripheral devices is based upon a priority scheme. The execution of an input/output instruction is included in the priority scheme. The hierarchy of priority (highest to lowest) is as follows:

	Peripheral Device	
Priority	Number (Decimal)	Address (Octal)
1	I/O Instructions	
2	0 – 7	00 – 07*
3	8 – 15	10 – 17
4	16 – 23	20 – 27
5	24 – 31	30 – 37
6	32 – 39	40 – 47
7	40 – 47	50 – 57
8	48 – 55	60 – 67
9	46 – 127	100 – 177
10	56 – 63	70 – 77

*Special I/O addresses, see table 4-1.

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4-4. Programmed I/O Communication Class

Input/output instructions enable the computer to provide control for I/O data communication.

a. *Input/Output Instructions.* I/O instructions have the following general characteristics:

(1) Executed in privileged program levels only.

(2) Timing is independent of the peripheral device; however, an indicator signal from the peripheral device is required within ten microseconds of the command sequence to indicate the acceptance of the command data or that data has been transmitted, otherwise the device time-out bit of the indicator register is set.

(3) A secondary CPU (without an IOU) executing an input/output instruction sets specification violation bit position 5 in the query register.

The programmed I/O communication is performed by the computer instructions specified in table 4-2.

b. *Device Command (DEV).* Execution of the DEV results in the following actions:

(1) The eight most significant bits (bit positions 16 to 23) of the instruction operand, as shown in figure 4-2, are transmitted to the peripheral device addressed by the eight least significant bits (bits 24 to 31) of the operand.

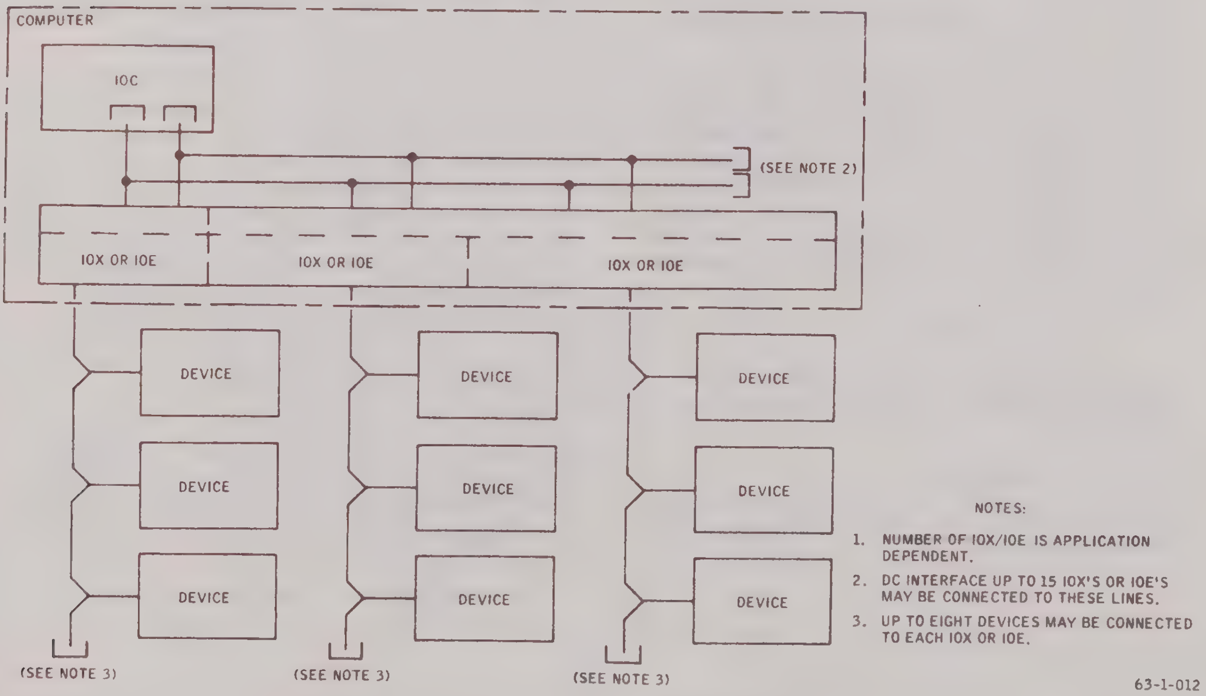
COMPUTER
IOC
(SEE NOTE 2)
IOX OR IOE
IOX OR IOE
IOX OR IOE
DEVICE
DEVICE
DEVICE
DEVICE
DEVICE
DEVICE
DEVICE
DEVICE
DEVICE
(SEE NOTE 3)
(SEE NOTE 3)
(SEE NOTE 3)
NOTES:
1. NUMBER OF IOX/IOE IS APPLICATION DEPENDENT.
2. DC INTERFACE UP TO 15 IOX'S OR IOE'S MAY BE CONNECTED TO THESE LINES.
3. UP TO EIGHT DEVICES MAY BE CONNECTED TO EACH IOX OR IOE.
63-1-012

Figure 4-1. I/O Interfaces Between the AN/GYK-12 Computer and the Peripheral Devices

(2) The H field of the instruction word is not used.

(3) All address modes are allowed.

NOTE

For instruction word format, refer to chapter 5.

c. *Device Command and Exit (DEX).* The DEX instruction operates the same as the DEV instruction (refer to paragraph 4-5a) with the following additions:

(1) The DEX instruction causes the status bit in the program activity register corresponding to the operating program to be reset.

(2) The level lock indicator in the query register is reset and a program level change occurs.

(3) When the level change (LC) indicator is set, only process register zero is saved.

d. *Input to Register (ITR).* The ITR instruction operates as follows:

Table 4-1. Special Input/Output Addresses and Associated Commands

Device Address (Octal)	Name	Device Command DEV or DEX	Input to Register (ITR)	Output from Register (OFR)	Key Termination Words
00	Secondary CPU interrupter/start[4]. I/O memory access control.	$(Y)_0$ = 1 Interrupt CPU 2; $(Y)_1$ = 1 Start CPU 2	- - -	Sets I/O memory access control bits	None
01	Monitor register	- - -	Read monitor register into specified process register	Set bits in monitor register[1]	None
02	Monitor register, and maintenance register	- - -	Read maintenance register into specified process register	Reset bits in monitor register[2]	Key word (0078) not used Termination word (007A) interrupt from monitor register
03	Real-time clock (RTC) 0	ON/OFF control of RTC 0, 1, and 2	- - -	- - -	Key word (007C) Termination word (007E)
04	RTC 1	- - -	- - -	- - -	Key word (00B8) Termination word (00BA)
05	RTC 2	- - -	- - -	- - -	Key word (00BC) Termination word (00BE)
06	CSIN (COMSEC)[3]	- - -	- - -	- - -	Key word (00E8) Termination word (00EA)
07	CSIN (COMSEC)[3]	- - -	- - -	- - -	Key word (00EC) Termination word (00EE)

[1] A one in bit position N of (H) sets a ONE in the corresponding bit position of the monitor register.

[2] A one in bit position N of (H) sets a ZERO in the corresponding bit position of the monitor register.

[3] Only used in TACFIRE.

[4] Only used in AN/TSQ-73.

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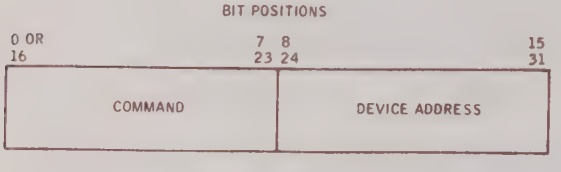
Table 4-2. AN/GYK-12 Computer I/O Instructions

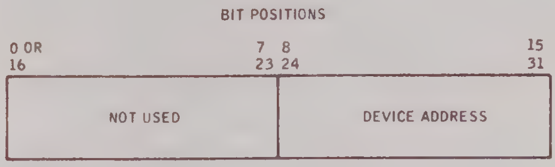
Acronym	Definition	General Purpose
DEV	Device command	Commands a peripheral device to perform one of its special functions, e.g., rewind a magnetic tape.
DEX	Device command and exit	Used as a DEV. Additionally the operating program level is terminated.
ITR	Input to register	Used to interrogate a status message from a peripheral device or to produce programmed input of a discrete word of one to four 8-bit bytes. (Parity is checked for each byte. At least one bit of each byte or the parity bit must be one.)
OFR	Output from register	Used to set indicators or to provide a programmed output of a discrete word of four 8-bit bytes, such as the starting address to a memory device. Parity is added to each byte.

70061-41



63-1-013

Figure 4-2. DEV and DEX Instruction Operand Format



63-1-014

Figure 4-3. ITR and OFR Instruction Operand Format

(1) The peripheral device addressed by the eight least significant bits of the instruction operand (see figure 4-3) transmits one to four, 8-bit bytes to the computer.

(2) The transmitted data is stored in the process register specified by the H field of the instruction.

(3) All address modes are allowed.

(4) The input parity error (IE) bit, in the indicator register, is set when parity is incorrect.

NOTE

For instruction word format refer to chapter 5.

e. *Output From Register (OFR).* The OFR instruction operates as follows:

(1) The eight least significant bit positions of the instruction operand select the peripheral device.

(2) The contents of the process register, addressed by the H field of the instruction word, are transmitted to the device as four 8-bit bytes.

(3) All address modes are allowed.

4-5. Automatic Input/Output (I/O) Communications Class

Automatic I/O communication is controlled by the contents of two I/O control words that are initially set by the computer program. The control words are the I/O keyword and the I/O termination word. Each of the 128 I/O station addresses, with the exception of the I/O memory access protect register (I/O station address 00-01), has an associated keyword and termination word. The keyword contains the mode of operation, the block length, and the data address in memory; it is used during each data word or byte transmission. The termination word is used at the end of a block of transferred data by device interrupt, or upon fault detection. It is used to specify status and program level to be activated at the completion of the I/O operation. One-hundred twenty-six keywords and one-hundred twenty-six termination words are stored in reserved locations of the base memory bank; each pair corresponding to a device address (see figure 4-1). Device addresses 0 thru 7 are reserved for special computer functions as specified in table 4-1. The remaining 120 station addresses are typically available for external devices.

Prior to an automatic input or output communication, the I/O control words must be initialized. The selected peripheral device must be prepared to transmit or receive as commanded by a DEV, DEX, or OFR instruction. The data communication then takes place at the rate of the peripheral device until the specified block length of data has been transferred. The termination word for this device is then used to indicate the status of the communication and the program level to be activated. Automatic I/O communication takes place at a rate not to exceed 400,000 words or bytes per second, and is independent of program execution. The determination of I/O communication, by word or by byte, is a function of the M field setting in the keyword.

NOTE

> I/O key and termination words are not related to program levels in the memory map.
>
> The key and termination words are further defined in paragraphs a and b below, respectively.

a. *Keyword.* The keyword contains three fields (see figure 4-4) to specify the block length set by mode bit or the transmission, the I/O mode of communication, and the current data memory address.

(1) BL, Block Length, Bit Positions 0-10. This bit field specifies the number of words (32-bits) or number of bytes (eight bits) in a block transmission or the number of time events in the alarm (clock) mode. A ZERO block length indicates the maximum block length of 2048 words, bytes or events. Blocks larger than 2048 words are obtained under the control of the peripheral device. For each data transfer or time event, the block length field is decremented. When this field is decremented to zero, the end-of-block (EOB) command is automatically sent to the peripheral device and the block transmission is terminated if the channel end bit in the termination word so specifies, or if the peripheral device initiates a device interrupt sequence after receiving the EOB command. If data transmission is discontinued by the peripheral device, then the peripheral device must initiate a device interrupt sequence to stimulate a program level change.

(2) M, Mode, Bit Positions 11-13. This three-bit field specifies one of the modes of operation in words or bytes as indicated in table 4-3.

(3) CA, Current Address, Bit Positions 14-31. This 18-bit field with bit positions 17 to 20 of the monitor register appended as more significant bits form a 22-bit address specify the half-word address of the memory location related to the current data transfer. For 32-bit word by byte transfers, the least significant bit is ignored.

b. *Termination Word.* The termination word is used to indicate conditions of transmission and to specify the program level to be activated at termination of a block data transmission or receipt of a device interrupt. Two program levels are shown, the normal (termination) program level and the error (termination) program level. The format of the termination word is as shown in figure 4-5.

(1) F, Block Complete, Bit Position 0. The F bit is set following the completion of a block of data transfer in word or byte modes. This is detected when the block length field of the associated keyword has been decremented from ONE to ZERO. The F bit is also set in the alarm (clock) mode when the block length field reaches ZERO. If the F bit is a ONE and bits E and R, are ZERO, it indicates that no error was detected during transmission or receipt of words or bytes.

Table 4-3. Modes of Operation

Mode Field (M) Octal	Mode of Operation
0	Inactive
1	Output, full word by bytes
2	Alarm (clock)
3	Input, full word by bytes
4	Output, upper byte in half word
5	Output, lower byte in half word
6	Input, upper byte in half word
7	Input, lower byte in half word

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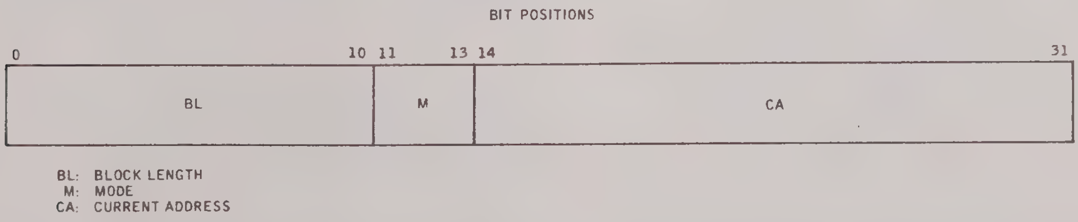

44-48-017

Figure 4-4. Input/Output Keyword Format

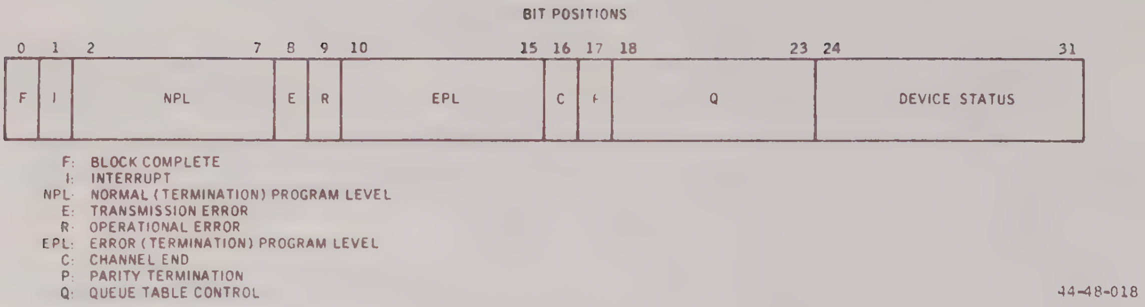

Figure 4-5. Termination Word Format

(2) I, Interrupt, Bit Position 1. The I-bit is set whenever an interrupt is received from a peripheral device. The indicator signal represents a device interrupt.

(3) NPL, Normal (Termination) Program Level, Bit Positions 2 to 7. This six-bit field defines the program level to be activated if the I bit of the termination word is set and the E and R bits are ZERO, or if the F bit of the termination word is set and the E and R bits are ZERO, and the channel end bit C is a ONE.

(4) E, Transmission Error, Bit Position 8. The E bit is set whenever the computer detects a parity error on the I/O communication network during an automatic data transfer operation.

(5) R, Operation Error, Bit Position 9. The R bit is set when:

(a) A request for service is received from a peripheral device and inactive mode 0 is stipulated in the keyword, and no Interrupt is received.

(b) A peripheral device fails to respond within ten microseconds when being serviced.

(c) A memory parity error occurs during access of keyword or data word.

(d) A memory access violation occurs.

(e) The computer does not service an active real-time clock within approximately one millisecond at its request.

NOTE

When the block-length field of the real-time clock zero is decremented to zero, then the mode field is automatically reset to zero.

(f) An output mode is specified in the keyword; input received and no indicator.

(6) EPL, Error (Termination) Program Level, Bit Positions 10 to 15. This six-bit field defines the program level to be stimulated if the I bit and the E bit are set and the R bit is ZERO; or if the F bit and E bit are set and the R bit is ZERO, and the channel end bit C is a ONE. See also (8) below for additional conditions.

(7) C, Channel End, Bit Position 16. The C bit controls the activation of the termination program level. When the C bit is set to ONE by software and the block length field of the associated keyword has been decremented from ONE to ZERO, the termination program level is activated. When the C bit is set to ZERO by software, the termination program level is not activated and normally the peripheral device will interrupt the computer with a subsequent indicator signal (multiple block length).

(8) P, Parity Termination, Bit Position 17. This bit, when set to a ONE by software, causes the error (termination) program level to be activated when a parity error is detected on the information lines in the automatic input mode. A device stop is sent to the peripheral device.

(9) Q, Queue Table Control, Bit Positions 18 to 23. When bit position 18 is ZERO, then bit positions 19 thru 23 are ignored and no action takes place. When bit position 18 is ONE, bit positions 19 thru 23 cause a bit to be set in the queue register corresponding to the termination program level. The bit position in the queue word is specified by bit positions 19 thru 23.

(10) Device Status, Bit Positions 24 to 31. The data on the information lines during a device interrupt sequence is stored into bit positions 24 to 31.

Section II. OPERATION

4-6. Modes of Operation

The M field of the I/O keyword determines the mode of control that the computer executes whenever it processes a request from a peripheral device. The modes of operation are discussed in the subsequent paragraphs.

a. *M = 0, Inactive Mode.* If the computer detects that the mode field is all ZEROS in the keyword, it sets the R-bit of the corresponding termination word, issues a stop signal to the peripheral device, and initiates a program level change to program level 2, unless an Interrupt is received.

b. *M = 2, Alarm (Clock) Mode.* In the alarm mode, the block length (BL) field of the keyword is decremented by one each time a request from a peripheral device is serviced. The current address (CA) field is not used, not modified and no data transmission occurs.

c. *M = 1 or 3, Full Word Output or Input.* These modes are for transmission of full 32-bit words, transmitted by four bytes plus parity. The BL field is decremented by one for each word transmitted or received. The CA field is incremented by two for each word transferred.

d. *M = 4 or 6, Upper Byte in Half Word Output or Input.* Data is transmitted or received as bytes, eight bits plus parity. This data is unpacked from the eight most significant bits in a 16-bit half word on output and packed into the eight most significant bits in a 16-bit half word on input, as addressed by the CA field. The CA field is not changed. The M field is automatically changed from 4 to 5 or 6 to 7 so that the next byte transmitted is the lower byte. The BL field is decremented by one.

e. *M = 5 or 7, Lower Byte in Half Word Output or Input.* Data is transmitted or received as bytes, eight bits plus parity. This data is unpacked from the eight least significant bits in a 16-bit half word on output and packed into the eight least significant bits in a 16-bit half word on input, as addressed by the CA field. The CA field is incremented by one and the M field is automatically changed from 5 to 4 or 7 to 6 so that the next byte transmitted is the upper byte. The BL field is decremented by one.

4-7. Types of Operation

When the computer operates in the automatic I/O communication class, communication with peripheral devices is established by the following operations: block of words by bytes or bytes transmission (block transmission); alarm (clock) operation, device interrupt, bootstrap program load. The type of operation is determined by the keyword or the peripheral device via transmitted control signals.

a. *Block Transmission.* Block transmission is a type of I/O operation where blocks of words or bytes are transmitted singly or in distinct groups and is activated by the following actions in the sequence specified.

(1) A DEV, DEX, or OFR instruction may signal the interface buffer of a peripheral device to transmit or receive data. The program loaded keyword will determine the block length, mode, and data memory address which will be effective for the transmission of the data.

(2) The computer may accept a request for a service signal to transfer data from the peripheral device. The rate of such requests is determined by the capability of the peripheral device to handle the data.

(3) On acknowledgement of the request, the proper keyword may be obtained from memory, modified, and returned to memory. The word or byte is transferred within five microseconds if the associated memory banks are not being used for programmed operations.

(4) When the block length is decremented from one to zero, the termination word is accessed and the F bit is set to ONE. In addition, an end-of-block (EOB) command sequence is sent to the peripheral device. As a result of this action, termination of communication and stimulation of program level will occur if the channel end bit is set to ONE or if the peripheral device responds with a device interrupt sequence. If bit 18 in the termination word is set to ONE, (specifying queueing option), the queue table will be accessed prior to termination of communication. Abnormal conditions occurring during data transfer are indicated in the monitor register and displayed on the front panel and include the following:

(a) The E bit of the termination word is set when the computer detects a parity error on the I/O network during data transfer. Data transfer continues when the P bit is ZERO. When the P bit is ONE, a stop signal is sent to the peripheral and the EPL is stimulated.

(b) The R bit of the termination word is set, a transfer to program level 2 occurs and the computer transmits a stop signal to the peripheral device under the conditions listed in paragraph 4-5b(5).

NOTE

For instruction word format, refer to chapter 5.

b. *Alarm (Clock) Operation.* The alarm (clock) operation is the same as specified for block transmission except that data is not transmitted and the CA field is not used.

c. *Device Interrupt.* When the computer acknowledges a request for service and the indicator signal is active, the following actions occur:

(1) The I bit of the termination word is set.

(2) The program level specified by the NPL field is activated if the E and R bits are ZERO.

(3) The program level specified by the EPL is stimulated if the E bit is a ONE.

(4) The bit specified by the Q field of the termination word is set to a one in the QUEUE register of the activated program level specified by the NPL or EPL field if bit 18 of the termination word is a ONE.

d. *Bootstrap Program Load.* The computer has the ability to bootstrap program load with the depression of a pushbutton (see sections 4-13 and 4-14). A specified peripheral device will input a program into core memory and the central processing unit (CPU) will then perform a program level change to program level 63_{10} and begin program execution. When the button is pressed, the peripheral device associated with that channel is defined as the loading peripheral device. The loading sequence will begin upon release of the pressed button. The first action which occurs upon button release is the legend of the pressed button is illuminated. This notifies the operator that the computer is commencing a bootstrap program load. A master reset signal is sent to all peripheral devices (including program loading peripheral device); thus, all peripheral devices will be in a standby mode. This is also true for the real-time clocks. The CPU is stopped and no instructions will be accessed from memory until the bootstrap program load is accomplished.

NOTE

> The CPU is not master reset. If a CPU reset is desired, the operator should push the restart button on the front panel prior to pressing a program load button.

The IOC now sends a command to the loading peripheral device to cause it to send data to the computer. This command consists of one byte, 00001100_2. The loading peripheral device will begin to input data in its normal mode, that is, either by byte or word by byte. In either case, the IOC accepts the first byte of a group only. This means that in the case of a byte transmitting peripheral device, each byte is accepted. In the case of a word by byte transfer, only the first byte of a word is accepted. (This is true for the first seven transfers to the computer.) The first seven bytes of input to the computer will control the remainder of the program load function. These bytes define:

(1) Starting location for rest of load.

(2) Total number of words or bytes to load.

(a) A byte loading peripheral device can load 8192 words.

(b) A word-by-byte loading peripheral device can load 32, 768 words.

(3) Mode of input, byte or word by byte.

(4) The first seven bytes from the program loading peripheral device are presented in the following table.

Byte	Content	Check Byte and Reflected Check Byte
1	Check byte	MSB LSB [0 0 1 0 1 1 1 1]
2	Reflected check byte	MSB LSB [1 1 0 1 0 0 0 0]
3-6	Key word	
7	Block length extension	Most significant four bits of the byte

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Byte 1 is a check byte while byte 2 is reflected check byte. Byte 1 should always contain the value $2F_{16}$ and byte 2 should always contain the value $D0_{16}$ (the complement of $2F_{16}$). The two bytes are used by the IOC in automatic diagnostic checks to determine if I/O data transmissions are correct. Bytes 3 thru 6 form the keyword to be used by the IOC to control the remaining program load input past byte 7. Byte 3 is the most significant byte while byte 6 is the least significant byte. Byte 7 loads a block-length extension register (used only in bootstrap-program load) to enable to loading of more than 2048 words or bytes. An end-of-block (EOB) signal is not sent to the loading peripheral device until the keyword block length field and extension register goes to ZERO. The keyword is maintained in a hardware register rather than core during program load. Thus, the base memory location associated with the loading peripheral device may be loaded without altering the loading process. Upon completion of the program load input the CPU performs an automatic diagnostic check, and the computer makes a program level change to program level 63_{10} and begins accessing instructions. The light associated with the bootstrap button is not automatically extinguished, but must be programmed off by resetting the appropriate bit of the monitor register. While in program level 63_{10}, error exists (to program level 2) or I/O termination exits will not be honored. This effective level lock is reset once a program initiated exit from program level 63_{10} occurs. In the case of a pending error exit to program level 2, the flag bits of the indicator and query register are set, the program will not enter level 2; however, the indicator will remain set. In the case of an I/O interrupt while in program level 63_{10} the program activity register (PAR) status bit remembers the interrupt and it will be honored once level 63_{10} exits. It should be noted that while I/O operations are not locked out while in program level 63_{10}, none should occur (unless commanded by program level 63_{10}) unless due to the master reset initially broadcast by the IOC.

NOTE

The loading peripheral device must input at least 2 data bytes (byte input mode) or 2 data word (word input mode) in addition to the first 7 input transfers.

4-8. Input/Output Memory Access Control

The I/O memory access control applies to memory data transfers associated with automatic I/O operations as follows:

a. I/O memory access control is defined by two control bits for each of the 64 pages of 2048 words per page within the memory addressing capability associated with automatic I/O operations. These two bits control memory access as indicated in table 4-4. When an access violation occurs, the computer does not access memory, it sets the appropriate bits in the monitor register and a transfer to program level 2 is initiated. The computer has read and write access to the keyword and termination word regardless of the access control bit configuration for the related portion of memory.

b. OFR instructions to special device address 00 loads the memory access control circuits; the least significant 16 bits of the selected process register define the memory access for each 2048-word page of the stipulated 8,192-word memory word address as shown in table 4-5; the remaining bits are unused. Note the effect of monitor register bit positions 17 to 20 on the memory word address.

c. The IOC data word addressing reach is 131,072 word addresses for each monitor register bit positions 17 to 20 setting. When using MCMUs the data memory addresses and memory access control are shifted according to the monitor register setting.

4-9. Real-Time Clocks

The real-time clocks are a function of hardware interval timers and programmed counters which operate in the alarm mode as follows:

a. Three device addresses, 3, 4, and 5 are assigned to these real-time clocks called RTC 0, RTC 1 and RTC 2.

b. The real-time clocks initiate service requests at intervals of 1024 ±0.2 microseconds when activated (8192 ±1.6 in NICS-TARE).

c. When the BL field of the keyword for clock RTC 0 is decremented to zero, the M field is set to ZERO.

d. When a real-time clock issues a request for service when the M field is ZERO, a program hang-up condition occurs and is indicated by the two following settings: the setting of the R bit of the associated termination word; the setting of bit 15 of the monitor register and automatic transfer to program level 2.

(1) *Real-time clocks on/off control.* Real-time clocks 0, 1, and 2 are assigned device addresses, 3, 4, and 5, respectively. These three real-time clocks are deactivated whenever a bootstrap program load is initiated or the power is turned off or master reset is generated or they are deactivated by a DEV to 03 with appropriate bits set. The occurrence of these real-time clocks is under program control. A device command (DEV) and device command exit (DEX) with device address 3, determines whether any or all of these clocks are to be active. After a clock is activated, the first request for service occurs no later than 1024 microseconds (8192 in NICS-TARE) and no sooner than one microsecond. The format of the instruction operand is as shown in figure 4-6; the fields are defined as follows:

Table 4-4. I/O Memory Access Control

I/O Memory Access Control Bits	Name	Action Permitted		Action Inhibited	
00	All access	Read	Write	-	-
01	Output only	Read	-	-	Write
10	Input only	*	Write	Read*	-
11	No access	-	-	Read	Write

*A read operation for the purpose of inserting a byte into memory is allowed with this control configuration.

70061-43

Table 4-5. I/O Memory Access Control Fields for OFR Instruction to Device Address

Monitor Register Bit Positions 17 to 20	Memory Word Address	Bit Positions of Selected Process Register								
		16	17	18	19	20 23	24 25	26 27	28 29	30 31
0000 0001	0 to 8K 128K to 136K	0	0	0	0	Not Used	Access control bits for first page of 2048 words	Access control bits for second page of 2048 words	Access control bits for third page of 2048 words	Access control bits for fourth page of 2048 words
0000 0001	8K to 16K 136K to 144K	0	0	0	1					
0000 0001	16K to 24K 144K to 152K	0	0	1	0					
0000 0001	24K to 32K 152K to 160K	0	0	1	1					
0000 0001	32K to 40K 160K to 168K	0	1	0	0					
0000 0001	40K to 48K 168K to 176K	0	1	0	1					
0000 0001	48K to 56K 176K to 184K	0	1	1	0					
0000 0001	56K to 64K 184K to 192K	0	1	1	1					
0000 0001	64K to 72K 192K to 200K	1	0	0	0					
0000 0001	72K to 80K 200K to 208K	1	0	0	1					
0000 0001	80K to 88K 208K to 216K	1	0	1	0					
0000 0001	88K to 96K 216K to 224K	1	0	1	1					
0000 0001	96K to 104K 224K to 232K	1	1	0	0					
0000 0001	104K to 112K 232K to 240K	1	1	0	1					
0000 0001	112K to 120K 240K to 248K	1	1	1	0					
0000 0001	120K to 128K 248K to 256K	1	1	1	1					

Note: K = 1,024. For monitor register (bit positions 17 to 20) 0010 through 1111 add 128K to memory word address for each increment.

8K = 8,192
128K = 131,072 etc.

70061-44

BIT POSITIONS IN HALF WORD

0 16				4 20				8 24 15 31
ON				OFF				DEVICE ADDRESS
R T C 0	R T C 1	R T C 2		R T C 0	R T C 1	R T C 2		(BINARY 00000011)

A44-48-019

Figure 4-6. Real-Time Clock Activity Control Command Format

(a) The ON control bit positions 16, 17, and 18 control the activation of real-time clocks 0, 1, and 2. If the bit is a ONE, the clock will be activated; if the bit is a ZERO, it will be ignored.

(b) The OFF control bit positions 20, 21, and 22 control the deactivation of real-time clocks 0, 1, and 2. If the bit is a ONE, the clock will be deactivated; if the bit is a ZERO, it will be ignored.

(c) Device address 03 must be in bits 24 to 31, see table 4-1.

(2) *Real-time clock operation.* The real-time clocks operate in the automatic input/output communication class and are controlled by the key word and termination word. Both control words are to be initialized by the program prior to the activation of the clocks by a device command instruction. The block length in the key word contains the number of time events (1024 microsecond intervals) (8192 microseconds in NICS-TARE) to be counted. The mode field is 2. The current address field is not used. The termination word contains the program level to be activated when the block length is decremented to zero. If the computer fails to process a request for service (interval counting) from a real-time clock within 256 microseconds (2048 microseconds in NICS-TARE), a time-out error results. This time-out error causes the audible alarm (optional) and an indicator light on the front panel to be activated. Bit 14 of the monitor register (IOC time out) is set and an automatic transfer to program level 2 occurs.

4-10. Typical Peripheral Device Operation

Use of the interface between the computer and its peripheral devices is dependent upon the functions to be performed by the peripheral device(s) and the instructions the device(s) receive from the computer. Functions performed by the computer and the peripheral devices, as a result of interface are: DEV or DEX command; OFR command, ITR command, an automatic I/O (A), external interrupt (1), end of block (EOB), stop signal. The functions specified may be used in any combination. However, certain conventions should be observed. For example, an automatic input or output requires that the software in the CPU has set up a keyword and a termination word in the base memory. Otherwise, the I/O communication could fail because of an improperly specified mode, block length, or memory address in the keyword. Some typical sequences of these functions are as follows:

a. *DEV Sequence.* The computer commands a peripheral device to perform specified function, such as magnetic tape to rewind or to close a contact.

b. *DEV-I.* The computer commands a peripheral device to perform specified function, such as a magnetic tape to rewind. The peripheral device interrupts the computer when the function is performed.

c. *DEV-ITR.* The computer commands a peripheral device to perform specified function, such as turn on motor in a punch. Status of peripheral device is interrogated with ITR.

d. *DEV-A-DEV.* The computer commands a peripheral device to perform specified function such as paper tape punch to punch data on tape. Data is automatically exchanged between memory and the peripheral device. The computer can stop the tape punch with the second DEV, which can override the first command.

e. *DEV-A-Stop.* An automatic input or output operation is stopped by the computer when it detects certain error conditions. The peripheral device resets its logic.

f. *DEV-A-I.* A peripheral device operating in the automatic input mode and using variable length formats may recognize a special character such as end-of-message (EOM), it can notify the software in the computer with an interrupt.

g. *DEV-A-EOB.* When the computer commands a peripheral device to input or output a fixed length message, it notifies the peripheral device with an end-of-block (EOB) signal when the last byte is exchanged during the automatic transfer. The EOB signal will notify the software in the computer with a program interrupt if the C bit of the terminate word is a ONE.

h. *A.* The peripheral device inputs or outputs data automatically. When this mode is used singularly, the appropriate software must provide reinitiation of the keyword before the next block transfer takes place. It is recommended that a DEV-A-I or DEV-A-EOB sequence be used instead of an A operation only.

i. *OFR.* The computer commands a peripheral device to perform specified functions or to set up discrete settings in a peripheral device.

j. *OFR-A-EOB.* Computer commands a peripheral device to perform a specific function such as to write data on a memory device. The OFR includes the starting address or block address in the peripheral device. The peripheral device automatically writes the data until the computer transmits the EOB signal.

k. *OFR-A-I.* The peripheral device performs the commanded function. Upon completion, it interrupts the computer signifying the completion.

l. *OFR-I-DEV-A-EOB.* The computer commands a memory device to perform a seek operation. Completion of the seek operation is indicated with an external interrupt. The computer then commands the peripheral device to perform a write function. The automatic data output function is completed with an EOB.

m. *ITR.* The computer inputs a single word from a peripheral device which can be used to interrogate the status of the peripheral device or to input discrete data.

n. *I.* A single peripheral device, such as a switch contact, can interrupt the computer.

o. *I-ITR.* The peripheral device interrupts the computer. The computer can interrogate the peripheral device with an ITR to determine the reason for interruption.

4-11. Peripheral Device Options

During the transfer of data, several options may be used by the peripheral devices to activate different program levels. These options are: the channel-end option, queue register option.

a. *The Channel-End Option.* The channel-end option bit in the termination word, when set to a ONE, is used to activate a program level when the block length in the keyword is decremented to ZERO. Peripheral devices which have the capability to transfer data in larger blocks than 2,048 will use the option with C equal to ZERO. The peripheral device will activate the program level with an interrupt after receiving a preset number of EOB signals from the computer. Each time the computer decrements the block length to ZERO, it will send an EOB to the peripheral device. Peripheral devices may also be designed to use the option with C equal to ZERO for single or multiple block transfers when the peripheral devices use time after the last data transfer and before being available for the next operation: for example, when a magnetic tape has stopped or a peripheral device has to perform error checking after the last data has been transferred.

b. *Queue-Register Option.* The queue-register option is used when several peripheral devices have to be assigned to activate the same program level. The peripheral devices can be identified by setting of the selected bit in the queue register. The activated program level can test the queue register with the test and conditionally reset/skip instruction.

Section III. DIAGNOSE FEATURES

This section is subdivided to show the differences in diagnose features that depend upon the application. The subsections to follow are applicable to:

A. TACFIRE

B. AN/TSQ-73

C. AN/TTC-39

D. NICS-TARE

NOTE

The page numbers of the following subsections employ a capital letter reflecting the specific system as indicated above.

Section IIIA. DIAGNOSE FEATURES (TACFIRE)

4-12A. Diagnose Logic (TACFIRE)

The TACFIRE computer is a single Central Processing Unit (CPU) Input Output Unit (IOU) system. The diagnose functions are described below.

Built-in error detection and isolation hardware has been incorporated into the computer design. The incorporation of this hardware provides the computer with a built-in, self-test capability. This self-test hardware will function automatically when the computer undergoes bootstrap program load.

Figure 4-IIIA-1 shows the Program Load and Diagnose Control and Indicators that are located on the front panels of the IOU and the CPU, see figures 4-IIIA-2 and 4-IIIA-3. These front panels are described in detail in Section IVA. Bootstrap program load can be performed from two peripheral devices. The selection of the peripheral device is accomplished by pressing either of the PROGRAM LOAD pushbuttons, CHANNEL 10 or CHANNEL 11.

Bootstrap Program Load Operation self-test status is indicated to the operator via the DIAGNOSE STATUS on the CPU, see figure 4-IIIA-1. The successful completion of the built-in, self-test indicates that the computer is able to perform basic functions and that the bootstrap program is in memory.

The IOU can bootstrap program load from two peripheral devices see figure 4-IIIA-1. The desired peripheral device is selected by either pressing pushbutton CHANNEL 10 or CHANNEL 11. These are momentary action switches. Upon release of the pushbutton, the Input Output Control (IOC) is directed to the bootstrap program load mode. When the IOC enters this mode, pressed pushbutton is then illuminated. At this point, the CPU is stopped (not reset) and CPU DIAGNOSE STATUS indicator lights 1 through 18 and both PROGRAM LOAD STATUS indicators CPU and IOU, are illuminated. The IOC broadcasts a master reset to all peripheral devices followed by a DEV command byte 00001100_2 to the selected peripheral device (channel 10 or 11).

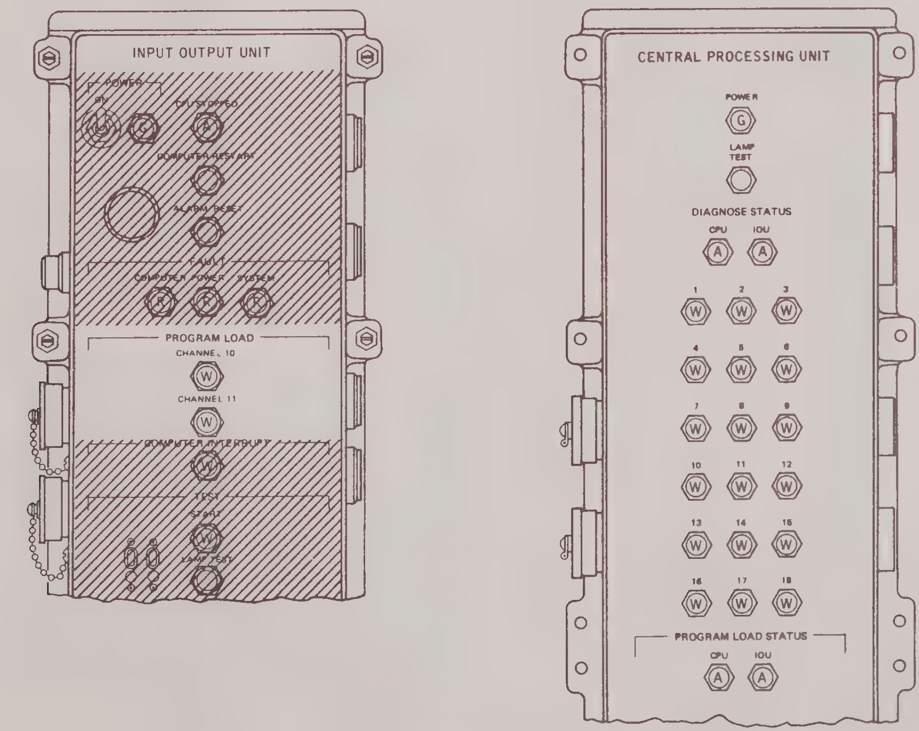
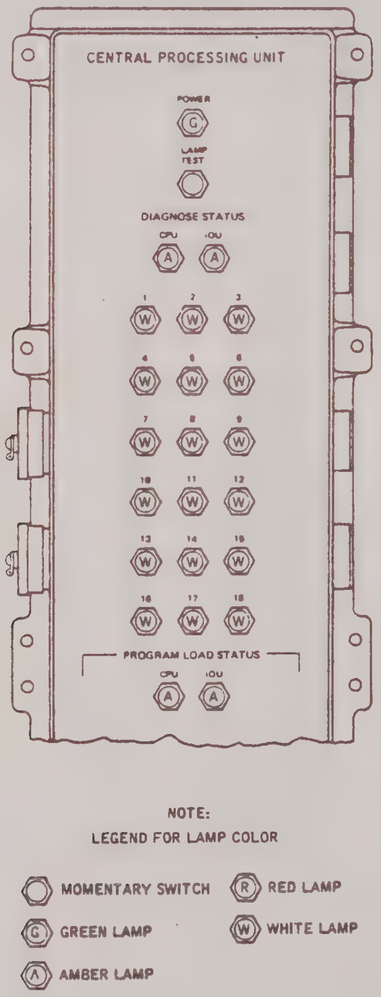

INPUT OUTPUT UNIT
POWER
ON
CPU STOPPED
A
G
COMPUTER RESTART
ALARM RESET
FAULT
COMPUTER
POWER
SYSTEM
R
PROGRAM LOAD
CHANNEL 10
W
CHANNEL 11
COMPUTER INTERRUPT
TEST
START
LAMP TEST
CENTRAL PROCESSING UNIT
POWER
LAMP TEST
DIAGNOSE STATUS
CPU
IOU
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
PROGRAM LOAD STATUS
70061-200

Figure 4-IIIA-1. Program Load and Diagnose Control and Indicators (TACFIRE)

The bootstrapping peripheral device, upon recognizing the command, starts inputting data to the computer. When an input parity error has been detected, the IOC will stop and the monitor register bit position 8 will be set, which illuminates the I/O CHANNEL FAULT indicator, PARITY. The peripheral device address is displayed on the three DATA EXCHANGE CHANNEL INDICATORS and the three DEVICE CHANNEL indicators. The peripheral device address consists of two octal digits (3 bits each). The least significant peripheral device octal digit illuminates the device channel lights, and the more significant octal digit illuminates the data exchange channel lights (bit positions 25 to 31 in the monitor register). Device response time out and memory time out will hang up the IOC; I/O CHANNEL FAULT indicator (TIMEOUT) and MEMORY FAULT indicator (TIMEOUT) will illuminate. I/O memory access violation and I/O memory parity errors are ignored (store operations).



44-48-020

Figure 4-IIIA-2. Diagnose Panel (TACFIRE)

The first seven bytes of input to the computer control the remaining bootstrap input as shown in the following table.

Byte	Content	Check Sum and Reflected Check Sum
1	Check sum	MSB LSB [0 0 1 0 1 1 1 1]
2	Reflected check sum	MSB LSB [1 1 0 1 0 0 0 0]
3-6	Key word	
7	Block length extension (most significant four bits of the byte)	

70061-702

Byte 1 is a check sum while byte 2 is a reflected check sum byte. Bytes 3 through 6 form the keyword to be used by the IOC. Byte 3 is the most significant byte while byte 6 is the least significant byte. Byte 7 loads a block-length extension register (used only in bootstrap program load).

NOTE

Numbers above each indicator light on the DIAGNOSE STATUS (figure 4-IIIA-1) are used for reference purposes in the corresponding text and do not appear on the actual panel.

Byte 1 enters the IOC in bit positions 23-31. The acceptance of byte 1 is determined by the IOC. If byte 1 is not entered correctly, DIAGNOSE STATUS indicator lights 10 and 11 will remain illuminated and the IOC hangs up. However, if byte 1 is entered correctly and the data comparison is correct, indicator lights 10 and 11 will be extinguished.

When byte 1 is correct, the IOC will accept byte 2 from the bootstrapping device. Acceptance or rejection of byte 2 is determined by the IOC. If byte 2 is not entered correctly, DIAGNOSE STATUS indicator lights 12 and 13 will remain illuminated and the IOC hangs up. However, when byte 2 is entered correctly and the data comparison is correct, indicator lights 12 and 13 will be extinguished.

When byte 2 is correct, the IOC will accept the next five bytes from the bootstrapping device; the IOC will assemble the five bytes into the keyword register and one byte into the block length extension register. The keyword is used to control the remainder of the bootstrap input.

NOTE

If the inputting device is the RAM, the mode field of the keyword should be normal-word input. If the device is the tape, the mode field should be normal-byte input.

The IOC, under keyword control, will accept the next byte or word from the bootstrapping device and place it in memory. When the IOC starts a memory-access cycle, DIAGNOSE STATUS indicator light 14 will be extinguished. However, when indicator light 14 remains illuminated, the memory-access cycle has not begun, and the IOC hangs up. When the memory cycle has been completed, indicator light 15 will be extinguished and the IOC will continue to input data from the bootstrapping device until the block-length register, including extension, goes to ZERO.

At this point, the IOC accesses the termination word from memory associated with the bootstrapping device. The contents of this location must be (D0D0D0D0)$_{16}$. The successful comparison of this location to the above bit configuration causes the DIAGNOSE STATUS indicator light 16 to be extinguished and PROGRAM LOAD STATUS IOU indicator is extinguished. When the comparison fails, indicator light 16 and PROGRAM LOAD STATUS IOU indicator light remain illuminated and the IOC hangs up.

When the comparison is successful, the IOC activates the CPU to begin operation. The CPU will now perform an automatic diagnostic, which is similar to the diagnose option 1 instruction explained in subparagraph 2 below. If a failure is detected during this sequence of checks, the CPU hangs up and DIAGNOSE STATUS indicator lights 17 and 18 and the PROGRAM LOAD STATUS CPU indicator light will remain illuminated. The other DIAGNOSE STATUS lights 1 through 16 remain unchanged.

When the forced diagnose option 1 passes successful, then DIAGNOSE STATUS light 17 is extinguished and the CPU undergoes a program level change to program level 63. The successful completion of this sequence indicates that the computer is able to perform basic functions and that the bootstrap program is loaded. Refer to subsequent paragraphs for the discussion of diagnose option 1 through 3 instructions.

a. *Diagnose Option 1.* The first instruction to be obeyed in program level 63 following the bootstrap

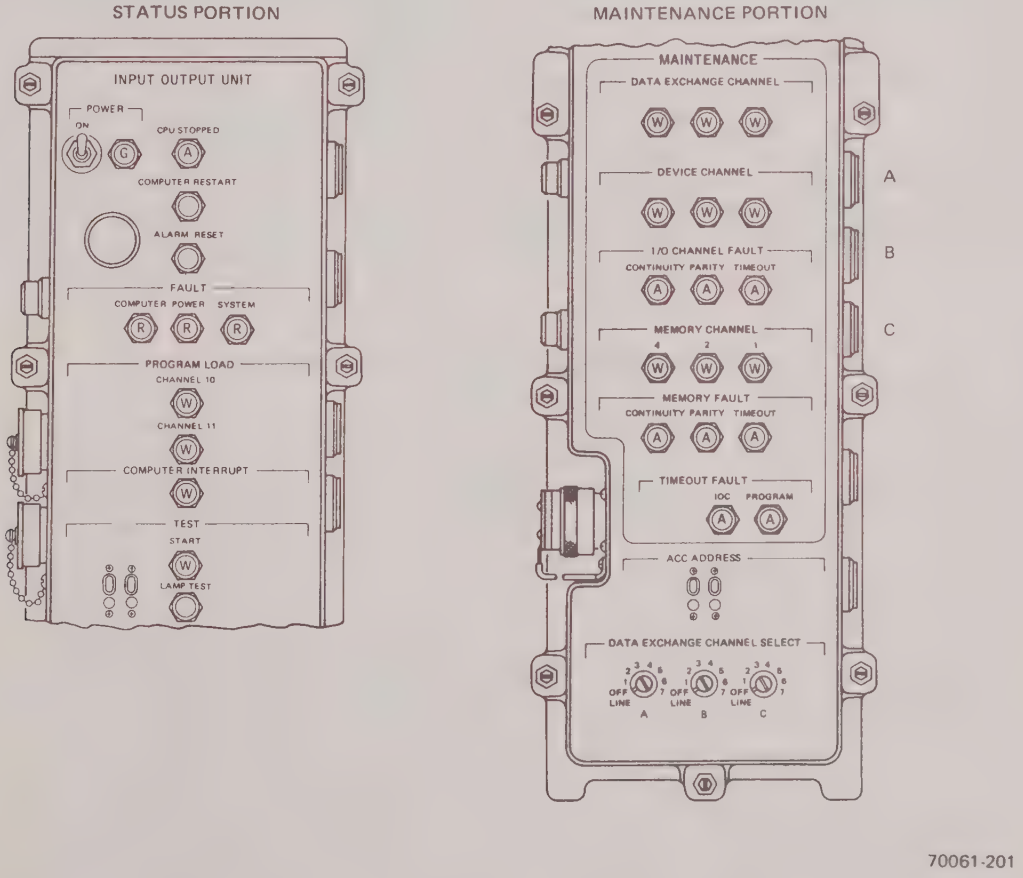

STATUS PORTION
INPUT OUTPUT UNIT
POWER
ON
G
CPU STOPPED
A
COMPUTER RESTART
ALARM RESET
FAULT
COMPUTER
POWER
SYSTEM
R
R
R
PROGRAM LOAD
CHANNEL 10
W
CHANNEL 11
W
COMPUTER INTERRUPT
W
TEST
START
W
LAMP TEST
MAINTENANCE PORTION
MAINTENANCE
DATA EXCHANGE CHANNEL
W
W
W
DEVICE CHANNEL
W
W
W
I/O CHANNEL FAULT
CONTINUITY
PARITY
TIMEOUT
A
A
A
MEMORY CHANNEL
4
2
1
W
W
W
MEMORY FAULT
CONTINUITY
PARITY
TIMEOUT
A
A
A
TIMEOUT FAULT
IOC
PROGRAM
A
A
ACC ADDRESS
DATA EXCHANGE CHANNEL SELECT
1 2 3 4 5 6 7
OFF LINE
A
B
C
A
B
C
70061-201

Figure 4-IIIA-3. Status and Maintenance Panel (TACFIRE)

sequence should be a diagnose option 1 instruction. See figure 4-IIIA-4 for the diagnose option 1 instruction format.

The diagnose option 1 instruction has operations similar to those performed in the forced diagnose sequence except that it is fetched from memory and its decode is out of the command (CC) register.

(1) If an error occurs during the execution of this instruction, the following will occur:

(a) DIAGNOSE STATUS indicator light 17 remains extinguished and light 18 remains illuminated.

(b) PROGRAM LOAD STATUS CPU remains illuminated.

(c) The CPU will halt and the DIAGNOSE STATUS lights remain unchanged; they can be used for further fault isolation.

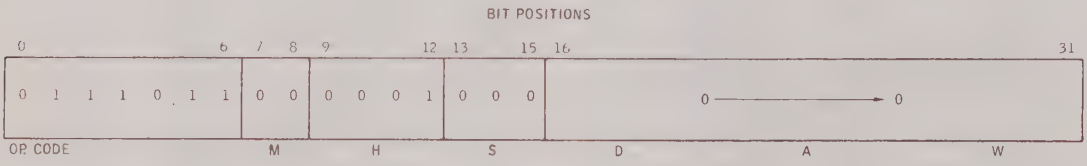
(2) If no error occurs, then the instruction's DAW field becomes the address of the next instruction. The DIAGNOSE STATUS lights remain unchanged and the PROGRAM LOAD STATUS CPU remains illuminated until a diagnose option 2 instruction is executed.

b. *Diagnose Option 2.* If no error is detected during the execution of diagnose option 1 instruction, the next instruction should be diagnose option 2 instruction. See figure 4-IIIA-5 for the diagnose option 2 instruction format. Bits 9, 10, and 16 thru 31 control the DIAGNOSE STATUS lights 17, 18, and 1 through 16 respectively (see figure 4-IIIA-1). A ZERO placed in bit position 10 of the instruction format will extinguish DIAGNOSE STATUS light 18 and also extinguish the PROGRAM LOAD STATUS CPU indicator. The execution of the diagnose option 2 instruction concludes the hardware diagnostic.

NOTE

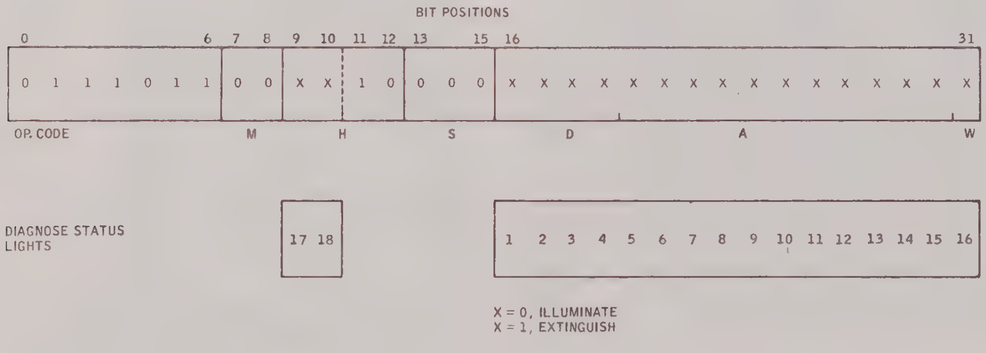
Bit position 10 in the diagnose option 2 instruction can only turn off the PROGRAM LOAD STATUS CPU indicator, but never on. However, a ZERO or ONE, will affect DIAGNOSE STATUS light 18.

c. *Diagnose Option 3.* The software diagnostic program begins with the diagnose option 3 instruction. See figure 4-IIIA-6 for the diagnose option 3 instruction format.


BIT POSITIONS
0
6
7
8
9
12
13
15
16
31
0 1 1 1 0 1 1
0 0
0 0 0 1
0 0 0
0 → 0
OP. CODE
M
H
S
D
A
W

63-1-046

Figure 4-IIIA-4. Diagnose Option 1 Instruction Format


BIT POSITIONS
0
6
7
8
9
10
11
12
13
15
16
31
0 1 1 1 0 1 1
0 0
X X
1 0
0 0 0
X X X X X X X X X X X X X X X X
OP. CODE
M
H
S
D
A
W
DIAGNOSE STATUS LIGHTS
17 18
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
X = 0, ILLUMINATE
X = 1, EXTINGUISH

70061-202

Figure 4-IIIA-5. Diagnose Option 2 Instruction Format

The software program may illuminate and extinguish the two DIAGNOSE STATUS lights labeled CPU and IOU. A ONE in bit position 30 will illuminate the DIAGNOSE STATUS CPU indicator; a ZERO will extinguish it. A ONE in bit position 31 will illuminate the DIAGNOSE STATUS IOU indicator; a ZERO will extinguish it.

The diagnose option 2 instruction can be used to extinguish or illuminate the DIAGNOSE STATUS lights 1 through 18 as shown in figure 4-IIIA-5.

It should be noted that during the software diagnostic, the CPU is still in program level 63. As long as the CPU stays in program level 63, the computer is in bootstrap program load which results in the following:

(1) Peripheral devices can be commanded to perform input or output operations.

(2) Peripheral device terminations or interrupts will be accepted; the status bit in the program activity register will be set, but program level changes are inhibited.

(3) Errors will not cause a program level change to program level 2.

Before exit from program level 63, the program should execute an OFR instruction to peripheral device address 02 with bit positions 3 and 4 in the selected process register being a ONE. These bits will reset the corresponding bits in the monitor register and extinguish the PROGRAM LOAD indicators, CHANNEL 11 and CHANNEL 10, respectively.

When a program in program level 63 executes a call executive program level and link (TXP), or call program level and link (TCP), or tie program level and link (TIE), or test and conditionally reset/skip (TQR) (only when initiating a program level change), or device command and exit (DEX) instruction, then the program level change will take place. Thus, then the bootstrap program load has been completed. Program level changes are permitted and errors will cause a transfer to program level 2.

d. As previously mentioned, pressing either PROGRAM LOAD pushbutton CHANNEL 10 or CHANNEL 11, will stop the CPU, but not reset it. When bootstrap program load should encounter loading difficulties, it is advisable to master reset the CPU. The procedure includes the following steps:

(1) Press RESTART pushbutton (do not release).

(2) Press PROGRAM LOAD CHANNEL 10 or CHANNEL 11 pushbutton (do not release).

(3) Release RESTART pushbutton.

(4) Release PROGRAM LOAD pushbutton CHANNEL 10 or CHANNEL 11.

This procedure will reset the CPU and IOU as well as stopping the CPU before bootstrap program load begins.

Pressing and releasing of the START pushbutton alone will reset the CPU and restart the CPU in program level 1. If there is no program stored in program level 1, then the CPU may encounter error conditions.

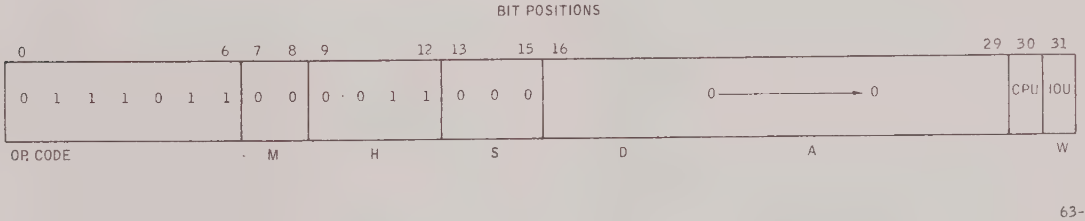


Figure 4-IIIA-6. Diagnose Option 3 Instruction Format

SECTION IIIB. DIAGNOSE FEATURES (AN/TSQ-73)

4-12B. Diagnose Logic (AN/TSQ-73)

The AN/TSQ-73 is a dual Central Processing Unit (CPU), single Input Output Unit (IOU) system. The two CPUs are called upper CPU and lower CPU. Either of these two CPUs can be selected by a switch to be the primary CPU. The other CPU automatically becomes the secondary CPU. The primary CPU (either upper or lower) is connected to the IOU.

All peripheral devices are connected to the IOU. The displays are also connected to the Display Output Unit (DOU). The DOU provides a data transfer path between the memories and the displays.

The memories have four ports. The memory access priorities, from highest to lowest priority, assigned to the ports are IOU, upper CPU, lower CPU, DOU.

Built in error detection and isolation hardware has been incorporated into the computer design. The incorporation of this hardware provides the computer with a built-in, self-test capability. This self-test hardware will function automatically when the computer undergoes bootstrap program load.

Figure 4-IIIB-1 shows the Program Load and Diagnose Control and Indicators which are located on the Status Portion of the ADP Status and Control Panel, see figure 4-IIIB-2. The front panel is described in detail in Section IVB. Bootstrap program load can be performed from two peripheral devices. The selection of the peripheral device is accomplished by pressing either PROGRAM LOAD pushbutton, CHAN 10 or CHAN 11.

A discussion of the diagnose logic is presented in the subsequent paragraphs. Bootstrap program load operation and self-test status is indicated on the program load and diagnose control and indicators of the ADP status and control panel, figure 4-IIIB-1. The successful completion of the built-in self-test indicates that the computer is able to perform basic functions and that the bootstrap program is in memory.

The IOU can bootstrap program load from two peripheral devices see figure 4-IIIB-1. The desired peripheral device is selected by either depressing push button CHAN 10 or CHAN 11. These are momentary action switches. Upon the release of the pushbutton, the Input Output Control (IOC) is directed to the bootstrap program load mode. When the IOC enters this mode, then the depressed push button is illuminated. At this point the CPU is stopped (not reset), DIAGNOSE CODE is 777 777, and PROG LOAD STATUS indicators, IOU CPU, are illuminated. The IOC broadcasts a master reset to all peripheral devices followed by a DEV command byte 00001100$_2$ to the selected peripheral device (channel 10 or 11).

The bootstrapping peripheral device upon recognizing the command starts inputting data to the computer. When an input parity error has been detected, the IOC will stop and the monitor register bit position 8 will be set which illuminates the FAULT DEVICE ERROR indicator, PARITY; the peripheral device address is displayed in FAULT, DEVICE ADDRESS (bit positions 25 to 31 in the monitor register). Device response time out and memory time out will hang up the IOC; DEVICE ERROR indicators, PARITY/T-OUT, are illuminated. I/O memory access violation and I/O memory parity errors are ignored (store operations).

The first seven bytes of input to the computer control the remaining bootstrap input as shown in the following table:

Byte	Content	Check Sum and Reflected Check Sum
1	Check sum	MSB LSB [0 0 1 0 1 1 1 1]
2	Reflected check sum	MSB LSB [1 1 0 1 0 0 0 0]
3-6	Key word	
7	Block length extension (most significant four bits of the byte)	

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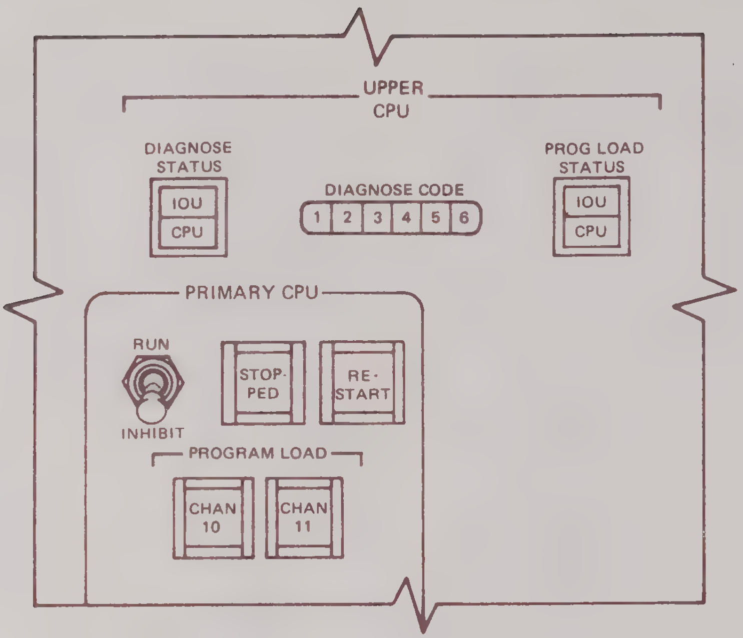
Byte 1 is a check sum while byte 2 is a reflected check sum byte. Bytes 3 through 6 form the keyword to be used by the IOC. Byte 3 is the most significant byte while byte 6 is the least significant byte. Byte 7 loads a block-length extension register (used only in bootstrap program load).

Byte 1 enters the IOC in bit positions 23-31. The acceptance of byte 1 is determined by the IOC. If byte 1 is not entered correctly, the DIAGNOSE CODE 777 777 or 777 377 is displayed. This code remains displayed and the IOC hangs up. However, when byte 1 is entered correctly and the data comparison is correct, then DIAGNOSE CODE 777 177 is displayed.

When byte 1 is correct, the IOC will accept byte 2 from the bootstrapping device. Acceptance or rejection of byte 2 is determined by the IOC. If byte 2 is not entered correctly, then 777 177 or 777 077 is displayed. This code remains displayed and the IOC hangs up. However, when byte 2 is entered correctly, and the data comparison is correct, then 777 037 is displayed.

When byte 2 is correct, the IOC will accept the next five bytes from the bootstrapping device; the IOC will assemble four bytes into the keyword register and one


UPPER CPU
DIAGNOSE STATUS
IOU
CPU
DIAGNOSE CODE
1 2 3 4 5 6
PROG LOAD STATUS
IOU
CPU
PRIMARY CPU
RUN
INHIBIT
STOP-PED
RE-START
PROGRAM LOAD
CHAN 10
CHAN 11

DIAGNOSE REGISTER BIT POSITIONS			DIAGNOSE CODE DIGIT POSITIONS
16	17	18	1
19	20	21	2
22	23	24	3
25	26	27	4
28	29	30	5
31	9	10	6

EXAMPLE:

DIAGNOSE REGISTER BIT POSITIONS:	9 10	16 17 18	19 20 21	22 23 24	25 26 27	28 29 30	31
DIAGNOSE BITS:	0 0	1 1 1	0 0 0	1 1 0	0 1 1	0 0 1	1
	4	7	0	6	3	1	
DIAGNOSE CODE:		7	0	6	3	1	4

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Figure 4-IIIB-1. Program Load and Diagnose Control and Indicators (AN/TSQ-73)

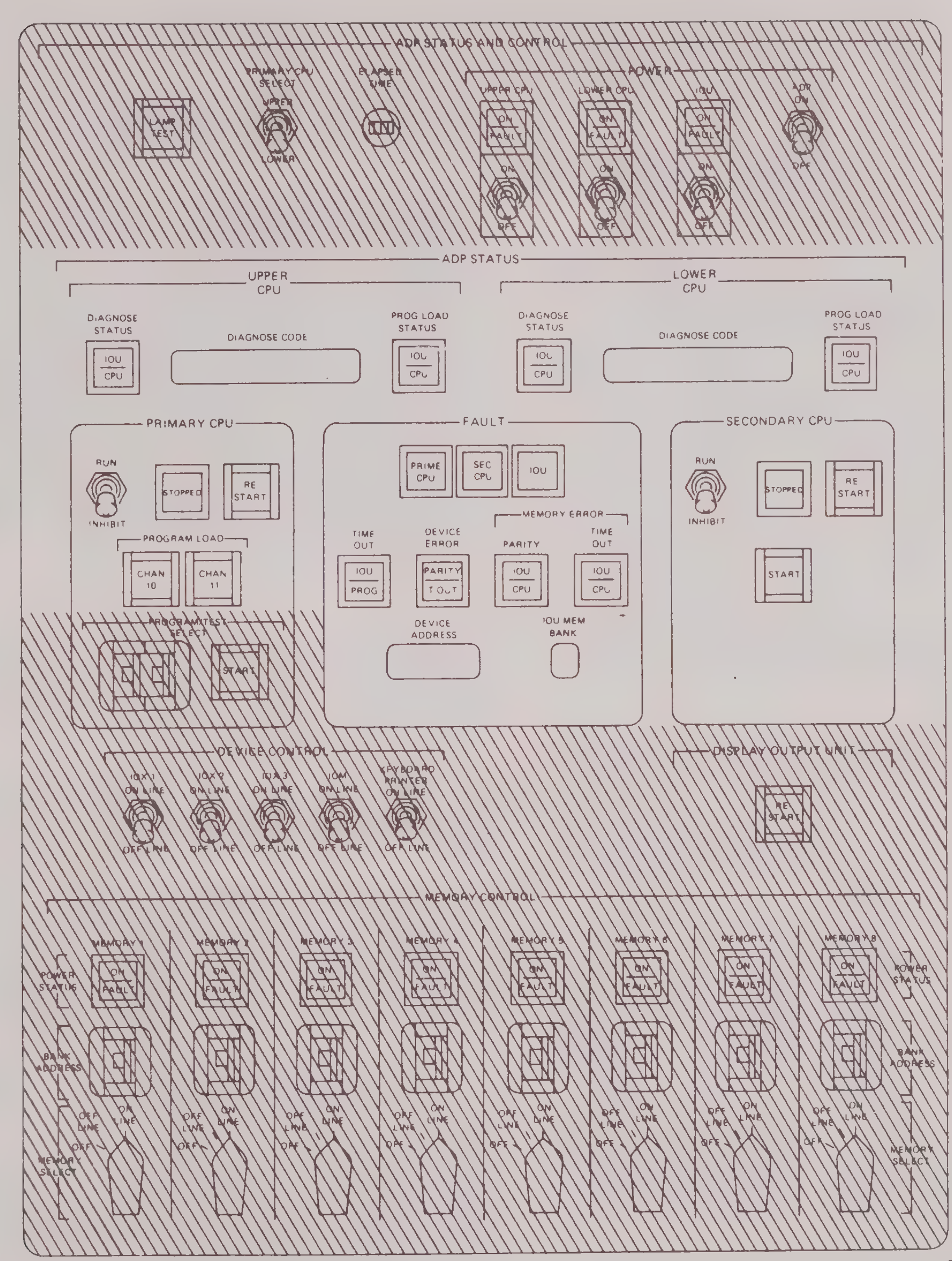
ADP STATUS AND CONTROL
LAMP TEST
PRIMARY CPU SELECT
UPPER
LOWER
ELAPSED TIME
POWER
UPPER CPU
LOWER CPU
IOU
ADP
ON
FAULT
ON
OFF
ADP STATUS
UPPER CPU
LOWER CPU
DIAGNOSE STATUS
DIAGNOSE CODE
PROG LOAD STATUS
IOU
CPU
PRIMARY CPU
RUN
INHIBIT
STOPPED
RE START
PROGRAM LOAD
CHAN 10
CHAN 11
PROGRAM TEST SELECT
START
FAULT
PRIME CPU
SEC CPU
IOU
MEMORY ERROR
TIME OUT
DEVICE ERROR
PARITY
TIME OUT
IOU PROG
PARITY T OUT
IOU CPU
DEVICE ADDRESS
IOU MEM BANK
SECONDARY CPU
RUN
INHIBIT
STOPPED
RE START
START
DEVICE CONTROL
IOX 1 ON LINE
IOX 2 ON LINE
IOX 3 ON LINE
IOM ON LINE
KEYBOARD PRINTER ON LINE
OFF LINE
DISPLAY OUTPUT UNIT
RE START
MEMORY CONTROL
MEMORY 1
MEMORY 2
MEMORY 3
MEMORY 4
MEMORY 5
MEMORY 6
MEMORY 7
MEMORY 8
POWER STATUS
ON
FAULT
BANK ADDRESS
OFF LINE
ON LINE
OFF
MEMORY SELECT
70061-204

Figure 4-IIIB-2. Status Portion of ADP Status and Control Panel

byte into the block length extension register. The keyword is used to control the remainder of the bootstrap input.

NOTE

> The mode field of the keyword should be full word input for both the DISC and TAPE bootstrap program load devices.

The IOC under keyword control will accept the next word from the bootstrapping device and place it in memory. When the IOC starts a memory cycle, then DIAGNOSE CODE 777 017 is displayed. However, when 777 037 remains displayed, then the IOC did not begin a memory cycle and the IOC hangs up. When a memory cycle has been completed, then 777 007 is displayed and the IOC will continue to input data from bootstrapping device until the block length register, including extension, goes to ZERO. At this point, the IOC accesses the termination word from memory associated with the bootstrapping device. The contents of this location must be $(D\,0\,D\,0\,D\,0\,D\,0)_{16}$. The successful comparison of this location to the above bit configuration causes 777 003 to be displayed and the PROG LOAD STATUS IOU indicator is extinguished. When the comparison fails, the 777 007 is displayed and the PROG LOAD STATUS IOU remains illuminated and the IOC hangs up.

When the comparison is successful, the IOC activates the CPU to begin operation. The CPU will not perform an automatic diagnostic which is similar to the diagnose option 1 instruction explained in subparagraph a below. If a failure is detected during this sequence of checks, the CPU hangs up and DIAGNOSE CODE XXX XX3 (X = 0 to 7) is displayed and the PROG LOAD STATUS CPU remains illuminated.

When the forced diagnose option 1 passes successfully, then 777 201 is displayed and the CPU undergoes a program level change to program level 63. The successful completion of this sequence indicates that the computer is able to perform basic functions and that the bootstrap program is loaded. Refer to the subsequent paragraphs for a discussion of diagnose option 1 through 3 instructions.

a. *Diagnose Option 1.* The first instruction to be obeyed in program level 63 following the bootstrap sequence should be a diagnose option 1 instruction. See figure 4-IIIB-3 for the diagnose option 1 instruction format.

The diagnose option 1 instruction has operations similar to those performed in the forced diagnose sequence except that it is fetched from memory and its decode is out of the command (CC) register.

(1) If an error occurs during the execution of this instruction, the following will occur:

(a) DIAGNOSE CODE will be XXX XX1 (X = 0 to 7).

(b) PROG LOAD STATUS CPU remains illuminated.

(c) The CPU will halt and the diagnose code remains unchanged; it can be used for further fault isolation.

(2) If no error occurs, then the instruction's DAW field becomes the address of the next instruction. The DIAGNOSE CODE remains unchanged and the PROG LOAD STATUS CPU remains illuminated until a diagnose option 2 instruction is executed.

b. *Diagnose Option 2.* If no error is detected during the execution of diagnose option 1 instruction, the next instruction should be diagnose option 2 instruction. See figure 4-IIIB-4 for the diagnose option 2 instruction format. Bits 9, 10 and 16 through 31 control the DIAGNOSE CODE (see figure 4-IIIB-1). A ZERO placed in bit position 10 of the instruction format will affect the least significant digit of the diagnose code and also extinguish the PROG LOAD STATUS CPU indicator. The execution of the diagnose option 2 instruction concludes the hardware diagnostic.

NOTE

> Bit position 10 in the diagnose option 2 instruction can only turn off the PROG LOAD STATUS CPU indicator, but never on. However, a ZERO, or ONE will affect the least significant DIAGNOSE CODE digit.

c. *Diagnose Option 3.* The software diagnostic program begins with the diagnose option 3 instruction. See figure 4-IIIB-5 for the diagnose option 3 instruction format.

The software program may illuminate and extinguish the two DIAGNOSE STATUS lights labeled CPU and IOU. A ONE in bit position 30 will illuminate the DIAGNOSE STATUS CPU indicator; a ZERO will extinguish it. A ONE in bit position 31 will illuminate the DIAGNOSE STATUS IOU indicator; a ZERO will extinguish it.

The diagnose option 2 instruction can be used to change the DIAGNOSE CODE as shown in figure 4-IIIB-1.

It should be noted that during the software diagnostic the CPU is still in program level 63. As long as the CPU stays in program level 63, the computer is in bootstrap program load which results in the following:

(1) Peripheral devices can be commanded to perform input or output operations.

(2) Peripheral device terminations or interrupts will be accepted; the status bit in the program activity register will be set, but program level changes are inhibited.

(3) Errors will not cause a program level change to program level 2.

Before exit from program level 63, the program should execute an OFR instruction to peripheral device address 02 with bit positions 3 and 4 in the selected process register being a ONE. These bits will reset the corresponding bit in the monitor register and extinguish the PROGRAM LOAD indicators, CHAN 11 and CHAN 10, respectively.

When a program in program level 63 executes a call executive program level and link (TXP), or call program level and link (TCP), or tie program level and link (TIE), or test and conditionally reset/skip (TQR) (only when initiating a program level change), or device command and exit (DEX) instruction, then the program level change will take place. Thus, then the bootstrap program load has been completed. Program level changes are permitted and errors will cause a transfer to program level 2.

d. As previously mentioned, pressing either PROGRAM LOAD pushbutton CHAN 10 or CHAN 11, will stop the CPU, but not reset it. When bootstrap program load should encounter loading difficulties, it is advisable to master reset the CPU. The procedure includes the following steps:

(1) Press RESTART pushbutton (do not release).

(2) Press PROGRAM LOAD pushbutton CHAN 10 or CHAN 11 (do not release).

(3) Release RESTART pushbutton.

(4) Release PROGRAM LOAD pushbutton CHAN 10 or CHAN 11.

This procedure will reset the CPU and IOU as well as stopping the CPU before bootstrap program load begins.

Pressing the releasing of the START pushbutton alone will reset the CPU and restart the CPU in program level 1. If there is no program stored in program level 1, then the CPU may encounter error conditions.

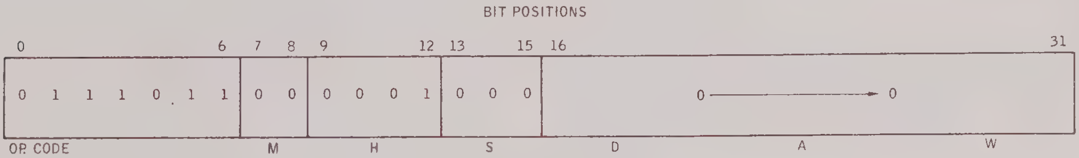
BIT POSITIONS
0
6
7
8
9
12
13
15
16
31
0 1 1 1 0 1 1
0 0
0 0 0 1
0 0 0
0 → 0
OP. CODE
M
H
S
D
A
W

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Figure 4-IIIB-3. Diagnose Option 1 Instruction Format

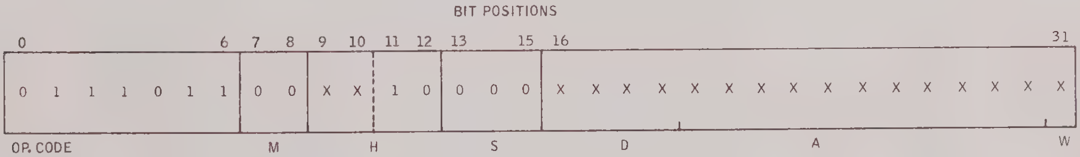
BIT POSITIONS
0
6
7
8
9
10
11
12
13
15
16
31
0 1 1 1 0 1 1
0 0
X X
1 0
0 0 0
X X X X X X X X X X X X X X X X
OP. CODE
M
H
S
D
A
W

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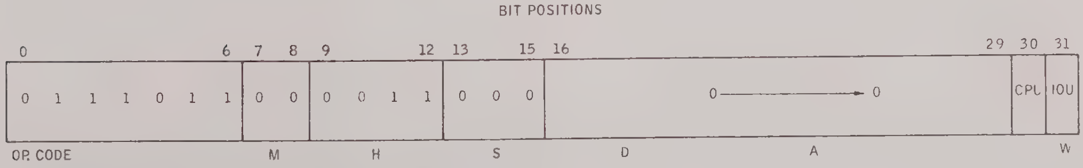
Figure 4-IIIB-4. Diagnose Option 2 Instruction Format


BIT POSITIONS
0
6
7
8
9
12
13
15
16
29
30
31
0 1 1 1 0 1 1
0 0
0 0 1 1
0 0 0
0 → 0
CPU
IOU
OP. CODE
M
H
S
D
A
W

63-1-048

Figure 4-IIIB-5. Diagnose Option 3 Instruction Format

Section IIIC. DIAGNOSE FEATURES (AN/TTC-39)

4-12C. Diagnose Logic (AN/TTC-39)

The AN/TTC-39 is a dual Central Processing Unit (CPU) Input Output Unit (IOU) system. Each computer (CPU, IOU, MEMORY) is connected to the same set of peripheral devices. The diagnose functions are identical in both computers and are independent of each other.

Built-in error detection and isolation hardware has been incorporated into the computer design. The incorporation of this hardware provides the computer with a built-in, self-test capability. This self-test hardware will function automatically when the computer undergoes bootstrap program load.

Figure 4-IIIC-1 shows the Program Load and Diagnose Control and Indicators which are located on the Status Portion of the ADP Status and Control Panel, see figure 4-IIIC-2. The front panel is discussed in detail in Section IVC. The 'Message Switch' of the AN/TTC-39 has rotary device select switch to select a peripheral device for bootstrap program load. The 'Circuit Switch' of the AN/TTC-39 has no rotary switch; bootstrap program load is performed only from one peripheral device.

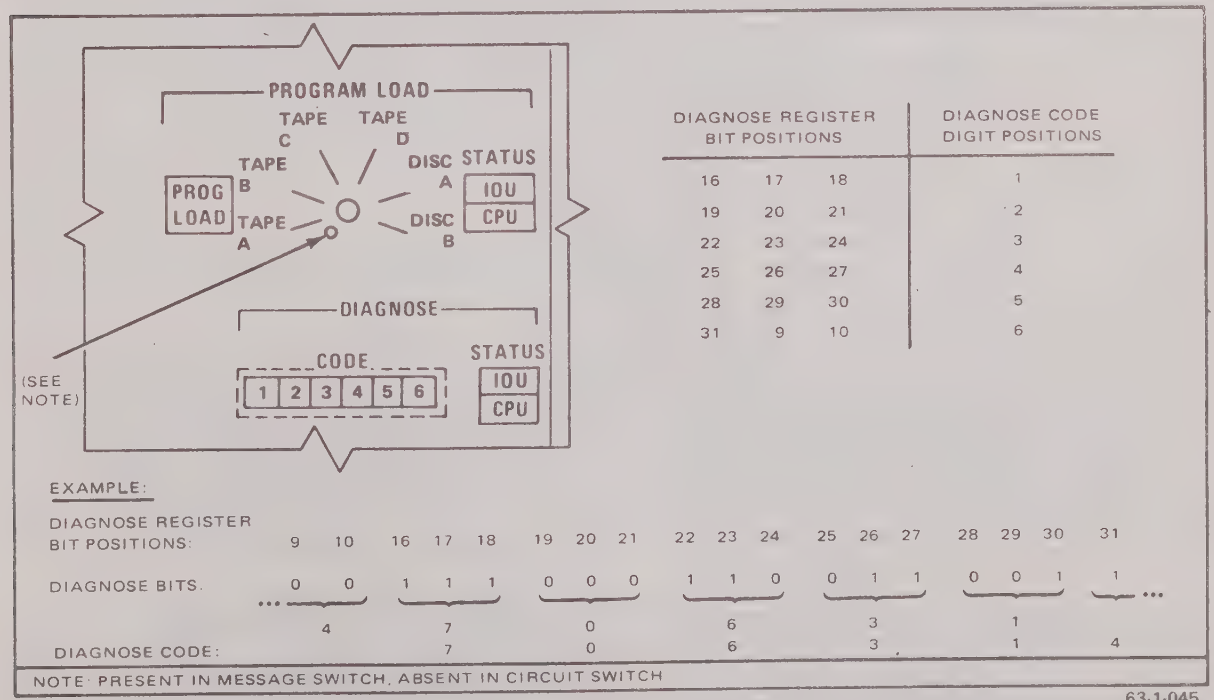
A discussion of the diagnose logic for the message switch is presented in the subsequent paragraphs.

Bootstrap program load operation and self-test status is indicated on the program load and diagnose control and indicators of the ADP status and control panel, figure 4-IIIC-1. The successful completion of the built-in self-test indicates that the computer is able to perform basic functions and that the bootstrap program is in memory.

The IOU can bootstrap program load from any one of six peripheral devices, see figure 4-IIIC-1. (Only one peripheral device for the circuit switch). There are two sets of peripheral device addresses for bootstrap program load.

For normal operation, the least significant PROGRAM TEST thumbwheel must show an even (E) number; then, the PROGRAM LOAD rotary switch selects the peripheral device connected to the IOE, which is one of the tapes or discs.

For system test operation, the least significant PROGRAM TEST thumbwheel can be dialed to an odd (0) number. Then the PROGRAM LOAD rotary switch selects the peripheral device connected to the IOX.



DIAGNOSE REGISTER BIT POSITIONS			DIAGNOSE CODE DIGIT POSITIONS
16	17	18	1
19	20	21	2
22	23	24	3
25	26	27	4
28	29	30	5
31	9	10	6

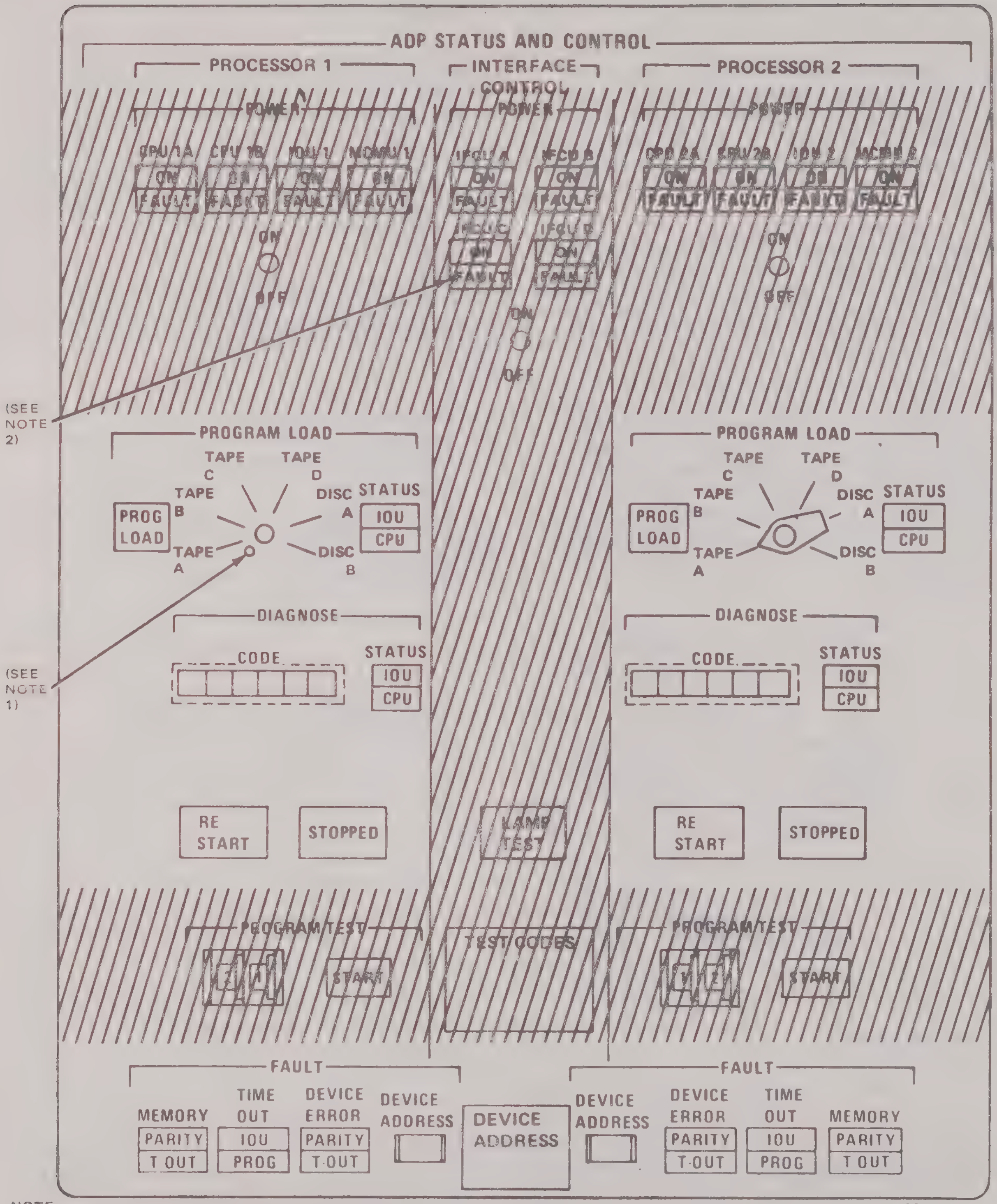
EXAMPLE:

DIAGNOSE REGISTER BIT POSITIONS:	9	10	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DIAGNOSE BITS.	0	0	1	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
	4		7			0			6			3			1			
DIAGNOSE CODE:			7			0			6			3			1			4

NOTE: PRESENT IN MESSAGE SWITCH, ABSENT IN CIRCUIT SWITCH

63-1-045

Figure 4-IIIC-1. Program Load and Diagnose Control and Indicators (AN/TTC-39)


ADP STATUS AND CONTROL
PROCESSOR 1
INTERFACE CONTROL
PROCESSOR 2
POWER
CPU 1A
CPU 1B
IOU 1
MCMU 1
ON
FAULT
IFCU A
IFCU B
IFCU C
IFCU D
CPU 2A
CPU 2B
IOU 2
MCMU 2
ON
OFF
(SEE NOTE 2)
PROGRAM LOAD
TAPE C
TAPE D
TAPE B
DISC A
TAPE A
DISC B
PROG LOAD
STATUS
IOU
CPU
(SEE NOTE 1)
DIAGNOSE
CODE
RE START
STOPPED
LAMP TEST
PROGRAM TEST
START
TEST CODES
FAULT
MEMORY
TIME OUT
DEVICE ERROR
DEVICE ADDRESS
PARITY
T OUT
IOU
PROG
T·OUT

NOTE: 1. PRESENT IN MESSAGE SWITCH, ABSENT IN CIRCUIT SWITCH.
2. FOUR IFCU IN MESSAGE SWITCH, ONE IFCU IN CIRCUIT SWITCH.

63-1-049

Figure 4-IIIC-2. Status Portion of ADP Status and Control Panel (AN/TTC-39)

The peripheral device addresses are as follows:

E/TAPE A = 10* or O/TAPE A = 30*
E/TAPE B = 11 O/TAPE B = 31
E/TAPE C = 12 O/TAPE C = 32
E/TAPE D = 13 O/TAPE D = 33
E/DISC A = 14 O/DISC A = 34
E/DISC B = 15 O/DISC B = 35

*Only for circuit switch

When the desired peripheral device is selected then the PROGRAM LOAD pushbutton, PROG LOAD, is pressed. This is a momentary action switch. Upon the release of the pushbutton, the Input Output Control (IOC) is directed to the bootstrap program load mode. When the IOC enters this mode, then PROG LOAD is illuminated. At this point the CPU is stopped (not reset), DIAGNOSE CODE is 777 777 and STATUS indicators, IOU CPU, are illuminated. The IOC broadcasts a master reset to all peripheral devices followed by a DEV command byte 00001100_2 to the selected peripheral device.

The bootstrapping peripheral device upon recognizing the command starts inputting data to the computer. When an input parity error has been detected, the IOC will stop and the monitor register bit position 8 will be set which illuminates the FAULT DEVICE ERROR indicator, PARITY; the peripheral device address is displayed in FAULT, DEVICE ADDRESS (bit positions 25 to 31 in the monitor register). Device response time out and memory time out will hang up the IOC; DEVICE ERROR indicators, PARITY/T-OUT, are illuminated I/O memory access violation and I/O memory parity errors are ignored (store operations).

The first seven bytes of input to the computer control the remaining bootstrap input as shown in the following table:

Byte	Content	Check Sum and Reflected Check Sum
1	Check sum	MSB LSB [0 0 1 0 1 1 1 1]
2	Reflected check sum	MSB LSB [1 1 0 1 0 0 0 0]
3-6	Key word	
7	Block length extension (most significant four bits of the byte)	

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Byte 1 is a check sum while byte 2 is a reflected check sum byte. Bytes 3 through 6 form the keyword to be used by the IOC. Byte 3 is the most significant byte while byte 6 is the least significant byte. Byte 7 loads a block-length extension register (used only in bootstrap program load).

Byte 1 enters the IOC in bit positions 23-31. The acceptance of byte 1 is determined by the IOC. If byte 1 is not entered correctly, the DIAGNOSE CODE 777 777 or 777 377 is displayed. This code remains displayed and the IOC hangs up. However, when byte 1 is entered correctly and the data comparison is correct, then DIAGNOSE CODE 777 177 is displayed.

When byte 1 is correct, the IOC will accept byte 2 from the bootstrapping device. Acceptance or rejection of byte 2 is determined by the IOC. If byte 2 is not entered correctly, then 777 177 or 777 077 is displayed. This code remains displayed and the IOC hangs up. However, when byte 2 is entered correctly, and the data comparison is correct, then 777 037 is displayed.

When byte 2 is correct, the IOC will accept the next five bytes from the bootstrapping device; the IOC will assemble four bytes into the keyword register and one byte into the block length extension register. The keyword is used to control the remainder of the bootstrap input.

NOTE

> The mode field of the keyword should be full word input for both the DISC and TAPE bootstrap program load devices.

The IOC under keyword control will accept the next word from the bootstrapping device and place it in memory. When the IOC starts a memory cycle, then DIAGNOSE CODE 777 017 is displayed. However, when 777 037 remains displayed, then the IOC did not begin a memory cycle and the IOC hangs up. When a memory cycle has been completed, then 777 007 is displayed and the IOC will continue to input data from bootstrapping device until the block length register (including extension) goes to ZERO.

At this point, the IOC accesses the termination word from memory associated with the bootstrapping device. The contents of this location must be $(D\ O\ D\ O\ D\ O\ D\ O)_{16}$. The successful comparison of this location to the above bit configuration causes 777 003 to be displayed and the STATUS IOU indicator is extinguished. When the comparison fails, the 777 007 is displayed and the STATUS IOU remains illuminated and the IOC hangs up.

When the comparison is successful, the IOC activates the CPU to begin operation. The CPU will now perform an automatic diagnostic which is similar to the diagnose option 1 instruction explained in subparagraph a below. If a failure is detected during this sequence of checks, the CPU hangs up and DIAGNOSE CODE XXX XX3 (X = 0 to 7) is displayed and the STATUS CPU remains illuminated.

When the forced diagnose option 1 passes successfully, then 777 201 is displayed and the CPU undergoes a program level change to program level 63. The successful completion of this sequence indicates that the computer is able to perform basic functions and that the bootstrap program is loaded. Refer to the subsequent paragraphs for a discussion of diagnose option 1 through 3 instructions.

a. *Diagnose Option 1.* The first instruction to be obeyed in program level 63 following the bootstrap sequence should be a diagnose option 1 instruction. See figure 4-IIIC-3 for the diagnose option 1 instruction format.

The diagnose option 1 instruction has operations similar to those performed in the forced diagnose sequence except that it is fetched from memory and its decode is out of the command (CC) register.

(1) If an error occurs during the execution of this instruction, the following will occur:

(a) DIAGNOSE CODE will be XXX XX1 (X = 0 to 7).

(b) STATUS CPU remains illuminated.

(c) The CPU will halt and the diagnose code remains unchanged; it can be used for further fault isolation.

(2) If no error occurs, then the instructions's DAW field becomes the address of the next instruction. The DIAGNOSE CODE remains unchanged and the STATUS CPU remains illuminated until a diagnose option 2 instruction is executed.

b. *Diagnose Option 2.* If no error is detected during the execution of diagnose option 1 instruction, the next instruction should be diagnose option 2 instruction. See figure 4-IIIC-4 for the diagnose option 2 instruction format. Bits 9, 10 and 16 through 31 control the DIAGNOSE CODE (see figure 4-IIIC-1). A ZERO placed in bit position 10 of the instruction format will affect the least significant digit of the diagnose code and also extinguish the STATUS CPU indicator. The execution of the diagnose option 2 instruction concludes the hardware diagnostic.

NOTE

> Bit position 10 in the diagnose option 2 instruction can only turn off the STATUS CPU indicator, but never on. However, a ZERO, or ONE will affect the least significant DIAGNOSE CODE digit.

c. *Diagnose Option 3.* The software diagnostic program begins with the diagnose option 3 instruction. See figure 4-IIIC-5 for the diagnose option 3 instruction format.

The software program may illuminate and extinguish the two DIAGNOSE STATUS lights labeled CPU and IOU. A ONE in bit position 30 will illuminate the DIAGNOSE STATUS CPU indicator; a ZERO will extinguish it. A ONE in bit position 31 will illuminate the DIAGNOSE STATUS IOU indicator; a ZERO will extinguish it.

The diagnose option 2 instruction can be used to change the DIAGNOSE CODE as shown in figure 4-IIIC-1.

It should be noted that during the software diagnostic the CPU is still in program level 63. As long as the CPU stays in program level 63, the computer is in bootstrap program load which results in the following:

(1) Peripheral devices can be commanded to perform input or output operations.

(2) Peripheral device terminations or interrupts will be accepted; the status bit in the program activity register will be set, but program level changes are inhibited.

(3) Errors will not cause a program level change to program level 2.

Before exit from program level 63, the program should execute an OFR instruction to peripheral device address 02 with bit position 4 in the selected process register being a ONE. This bit will reset the corresponding bit in the monitor register and extinguish the PROGRAM LOAD indicator, PROG LOAD.

When a program in program level 63 executes a call executive program level and link (TXP), or call program level and link (TCP), or tie program level and link (TIE), or test and conditionally reset/skip (TQR) (only when initiating a program level change), or device command and exit (DEX) instruction, then the program level change will take place. Thus, then the bootstrap program load has been completed. Program level changes are permitted and errors will cause a transfer to program level 2.

d. As previously mentioned, pressing the PROGRAM LOAD pushbutton, PROG LOAD; will stop the CPU, but not reset it. When bootstrap program load should encounter loading difficulties, it is advisable to master reset the CPU. The procedure includes the following steps:

(1) Press RESTART pushbutton (do not release).

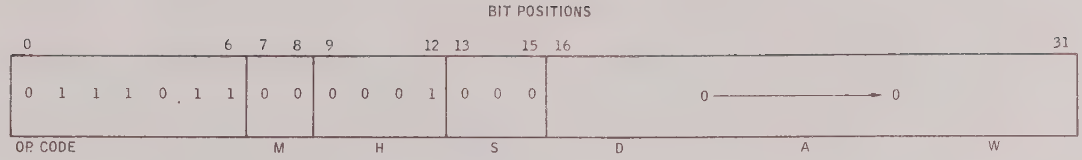
(2) Press PROG LOAD pushbutton (do not release).

(3) Release RESTART pushbutton.

(4) Release PROG LOAD pushbutton.

This procedure will reset the CPU and IOU as well as stopping the CPU before bootstrap program load begins.

Pressing and releasing of the START pushbutton alone will reset the CPU and restart the CPU in program level 1. If there is no program stored in program level 1, then the CPU may encounter error conditions.


BIT POSITIONS
0
6
7
8
9
12
13
15
16
31
0 1 1 1 0 1 1
0 0
0 0 0 1
0 0 0
0 → 0
OP. CODE
M
H
S
D
A
W

63-1-046

Figure 4-IIIC-3. Diagnose Option 1 Instruction Format

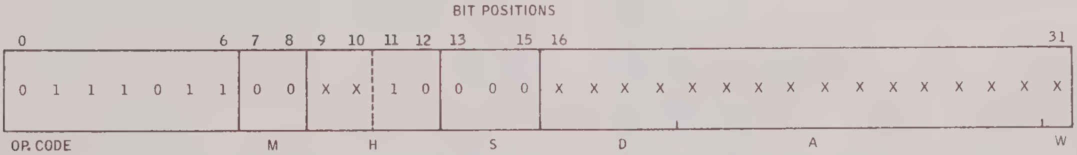

BIT POSITIONS
0
6
7
8
9
10
11
12
13
15
16
31
0 1 1 1 0 1 1
0 0
X X
1 0
0 0 0
X X X X X X X X X X X X X X X X
OP. CODE
M
H
S
D
A
W

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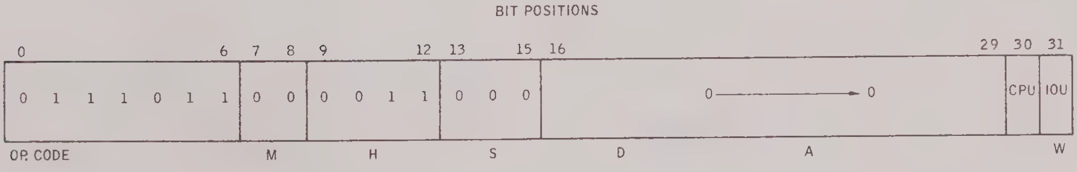
Figure 4-IIIC-4. Diagnose Option 2 Instruction Format


BIT POSITIONS
0
6
7
8
9
12
13
15
16
29
30
31
0 1 1 1 0 1 1
0 0
0 0 1 1
0 0 0
0 → 0
CPU
IOU
OP. CODE
M
H
S
D
A
W

63-1-048

Figure 4-IIIC-5. Diagnose Option 3 Instruction Format

Section IIID. DIAGNOSE FEATURES (NICS-TARE)

4-12D. Diagnose Logic (NICS-TARE)

The NICS-TARE is a dual Central Processing Unit (CPU) Input Output Unit (IOU) system. Each computer (CPU, IOU, MEMORY), is connected to the same set of peripheral devices. The diagnose functions are identical in both computers and are independent of each other.

Built-in error detection and isolation hardware has been incorporated into the computer design. The incorporation of this hardware provides the computer with a built-in, self-test capability. This self-test hardware will function automatically when the computer undergoes bootstrap program load.

Figure 4-IIID-1 shows the Program Load and Diagnose Control and Indicators which are located on the Status Portion of the ADP Status and Control Panel, see figure 4-IIID-2. The front panel is described in detail in Section IVD. A two position rotary switch selects Disc A or Disc B for bootstrap program load.

A discussion of the diagnose logic is presented in the subsequent paragraphs.

Bootstrap program load operation and self-test status is indicated on the program load and diagnose control and indicators of the ADP status and control panel, figure 4-IIID-1. The successful completion of the built-in self-test indicates that the computer is able to perform basic functions and that the bootstrap program is in memory.

The IOU can bootstrap program load from any one of two peripheral devices, see figure 4-IIID-1. There are five sets of peripheral device addresses for bootstrap program load.

For normal operation, the most significant PROGRAM TEST thumbwheel must show a ONE (1). Then the PROGRAM LOAD rotary switch selects the peripheral device connected to the IOE which is the Disc A or Disc B.

For system test operation, the most significant PROGRAM TEST thumbwheel can be dialed to 1, 4, 5, 6, or 7. Then the PROGRAM LOAD rotary switch selects the peripheral device connected to an IOE or the IOX.

The peripheral device addresses are as follows:

1/DISC A = 10*   1/DISC B = 11*   IOE #1
4/DISC A = 40   4/DISC B = 41   IOE #4
5/DISC A = 50   5/DISC B = 51   IOE #5
6/DISC A = 60   6/DISC B = 61   IOE #6
7/DISC A = 70   7/DISC B = 71   IOX #7

*Normal
operation

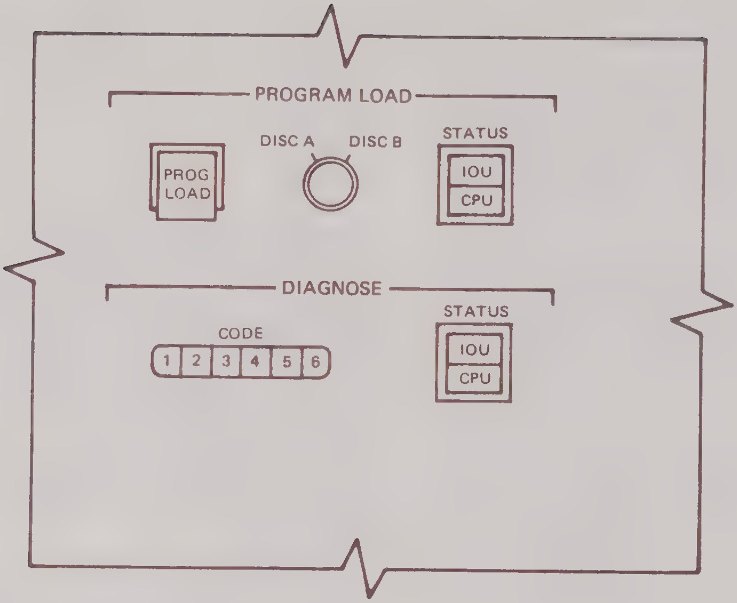
When the desired peripheral device is selected then the PROGRAM LOAD pushbutton, PROG LOAD, is pressed. This is a momentary action switch. Upon the release of the pushbutton, the Input/Output Control (IOC) is directed to the bootstrap program load mode. When the IOC enters this mode, then PROG LOAD is illuminated. At this point the CPU is stopped (not reset), DIAGNOSE CODE is 777 777 and STATUS indicators, IOU CPU, are illuminated. The IOC broadcasts a master reset to all peripheral devices followed by a DEV command byte 00001100_2 to the selected peripheral device.

The bootstrapping peripheral device upon recognizing the command starts inputting data to the computer. When an input parity error has been detected, the IOC will stop and the monitor register bit position 8 will be set which illuminates the FAULT DEVICE ERROR indicator, PARITY; the peripheral device address is displayed in FAULT, DEVICE ADDRESS (bit positions 25 to 31 in the monitor register). Device response time out and memory time out will hang up the IOC; DEVICE ERROR indicators, PARITY/T-OUT are illuminated. I/O memory access violation and I/O memory parity errors are ignored (store operations).

The first seven bytes of input to the computer control the remaining bootstrap input as shown in the following table:

Byte	Content	Check Sum and Reflected Check Sum
1	Check sum	MSB LSB [0 0 1 0 1 1 1 1]
2	Reflected check sum	MSB LSB [1 1 0 1 0 0 0 0]
3-6	Key word	
7	Block length extension (most significant four bits of the byte)	

70061-702


PROGRAM LOAD
PROG LOAD
DISC A
DISC B
STATUS
IOU
CPU
DIAGNOSE
CODE
1
2
3
4
5
6
STATUS
IOU
CPU

DIAGNOSE REGISTER BIT POSITIONS			DIAGNOSE CODE DIGIT POSITIONS
16	17	18	1
19	20	21	2
22	23	24	3
25	26	27	4
28	29	30	5
31	9	10	6

EXAMPLE:

DIAGNOSE REGISTER BIT POSITIONS	9	10	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
DIAGNOSE BITS:	0	0	1	1	1	0	0	0	1	1	0	0	1	1	0	0	1	1
	4			7			0			6			3			1		
DIAGNOSE CODE:				7			0			6			3			1		4

70061-205

Figure 4-IIID-1. Program Load and Diagnose Control and Indicators (NICS-TARE)

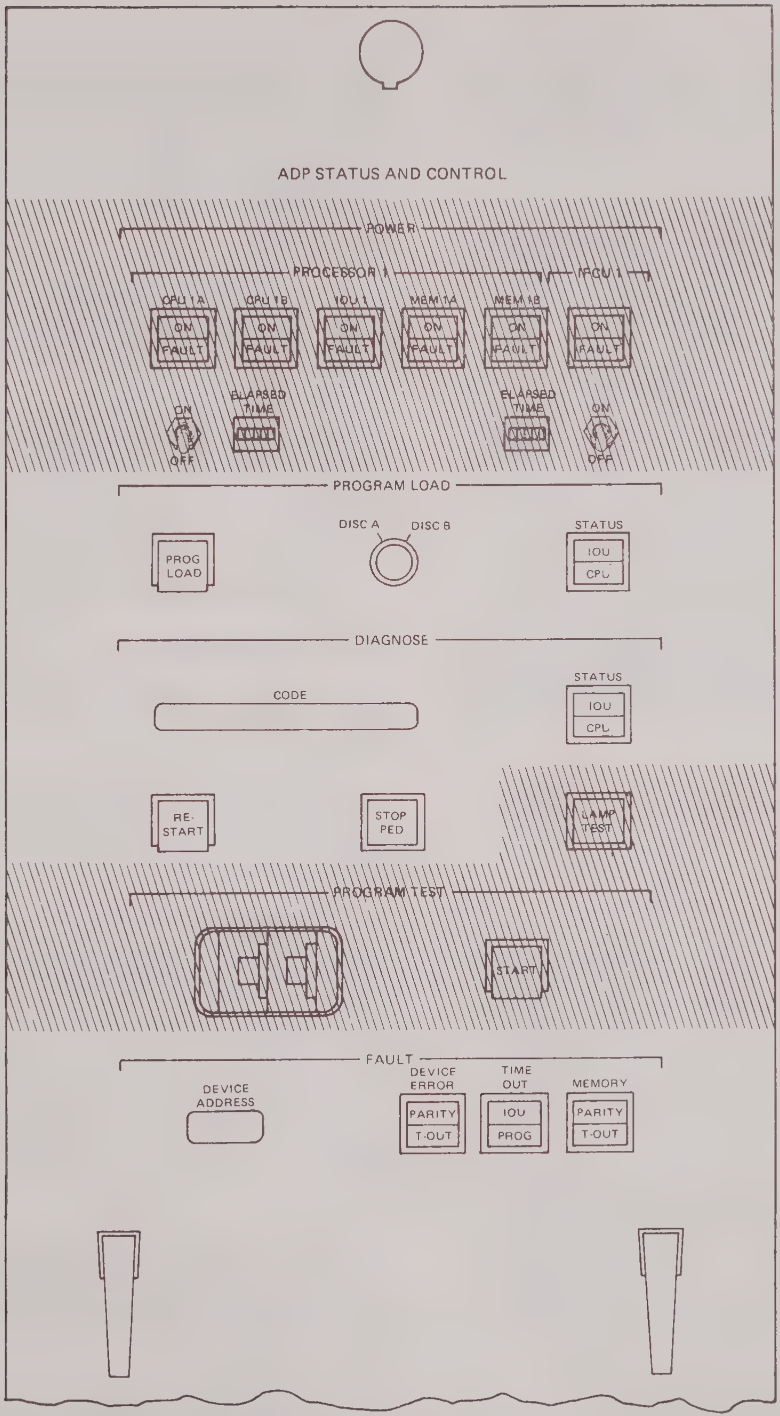

ADP STATUS AND CONTROL
POWER
PROCESSOR 1
IPCU 1
CPU 1A
CPU 1B
IOU 1
MEM 1A
MEM 1B
ON
FAULT
ON
FAULT
ON
FAULT
ON
FAULT
ON
FAULT
ON
FAULT
ON
OFF
ELAPSED TIME
ELAPSED TIME
ON
OFF
PROGRAM LOAD
PROG LOAD
DISC A
DISC B
STATUS
IOU
CPU
DIAGNOSE
CODE
STATUS
IOU
CPU
RE-START
STOP PED
LAMP TEST
PROGRAM TEST
START
FAULT
DEVICE ADDRESS
DEVICE ERROR
PARITY
T-OUT
TIME OUT
IOU
PROG
MEMORY
PARITY
T-OUT

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Figure 4-IIID-2. Status Portion of ADP Status and Control Panel (NICS-TARE)

Byte 1 is a check sum while byte 2 is a reflected check sum byte. Bytes 3 through 6 form the keyword to be used by the IOC. Byte 3 is the most significant byte while byte 6 is the least significant byte. Byte 7 loads a block-length extension register (used only in bootstrap program load).

Byte 1 enters the IOC in bit positions 23-31. The acceptance of byte 1 is determined by the IOC. If byte 1 is not entered correctly, the DIAGNOSE CODE 777 777 or 777 377 is displayed. This code remains displayed and the IOC hangs up. However, when byte 1 is entered correctly and the data comparison is correct, then DIAGNOSE CODE 777 177 is displayed.

When byte 1 is correct, the IOC will accept byte 2 from the bootstrapping device. Acceptance or rejection of byte 2 is determined by the IOC. If byte 2 is not entered correctly, then 777 177 or 777 077 is displayed. This code remains displayed and the IOC hangs up. However, when byte 2 is entered correctly, and the data comparison is correct, then 777 037 is displayed.

When byte 2 is correct, the IOC will accept the next five bytes from the boot-strapping device; the IOC will assemble four bytes into the keyword register and one byte into the block length extension register. The keyword is used to control the remainder of the bootstrap input.

NOTE

> The mode field of the keyword should be full word input for the DISC bootstrap program load devices.

The IOC under keyword control will accept the next word from the bootstrapping device and place it in memory. When the IOC starts a memory cycle, then DIAGNOSE CODE 777 017 is displayed. However, when 777 037 remains displayed, then the IOC did not begin a memory cycle and the IOC hangs up. When a memory cycle has been completed, then 777 007 is displayed and the IOC will continue to input data from boot-strapping device until the block length register (including extension) goes to ZERO. At this point, the IOC accesses the termination word from memory associated with the bootstrapping device. The contents of this location must be $(D\,O\,D\,O\,D\,O\,D\,O)_{16}$. The successful comparison of this location to the above bit configuration causes 777 003 to be displayed and the STATUS IOU indicator is extinguished. When the comparison fails, the 777 007 is displayed and the STATUS IOU remains illuminated and the IOC hangs up.

When the comparison is successful, the IOC activates the CPU to begin operation. The CPU will now perform an automatic diagnostic which is similar to the diagnose option 1 instruction explained in subparagraph a below. If a failure is detected during this sequence of checks, the CPU hangs up and DIAGNOSE CODE XXX XX3 (X = 0 to 7) is displayed and the STATUS CPU remains illuminated.

When the forced diagnose option 1 passes successfully, then 777 201 is displayed and the CPU undergoes a program level change to program level 63. The successful completion of this sequence indicates that the computer is able to perform basic functions and that the bootstrap program is loaded. Refer to the subsequent paragraphs for a discussion of diagnose option 1 through 3 instructions.

a. *Diagnose Option 1.* The first instruction to be obeyed in program level 63 following the bootstrap sequence should be a diagnose option 1 instruction. See figure 4-IIID-3 for the diagnose option 1 instruction format.

The diagnose option 1 instruction has operations similar to those performed in the forced diagnose sequence except that it is fetched from memory and its decode is out of the command (CC) register.

(1) If an error occurs during the execution of this instruction, the following will occur:

(a) DIAGNOSE CODE will be XXX XX1 (X = 0 to 7).

(b) STATUS CPU remains illuminated.

(c) The CPU will halt and the diagnose code remains unchanged; it can be used for further fault isolation.

(2) If no error occurs, then the instructions's DAW field becomes the address of the next instruction. The DIAGNOSE CODE remains unchanged and the STATUS CPU remains illuminated until a diagnose option 2 instruction is executed.

b. *Diagnose Option 2.* If no error is detected during the execution of diagnose option 1 instruction, the next instruction should be diagnose option 2 instruction. See figure 4-IIID-4 for the diagnose option 2 instruction format. Bits 9, 10 and 16 through 31 control the DIAGNOSE CODE (see figure 4-IIID-1). A ZERO placed in bit position 10 of the instruction format will affect the least significant digit of the diagnose code and also extinguish the STATUS CPU indicator. The execution of the diagnose option 2 instruction concludes the hardware diagnostic.

NOTE

> Bit position 10 in the diagnose option 2 instruction can only turn off the STATUS CPU indicator, but never on. However, a ZERO, or ONE will affect the least significant DIAGNOSE CODE digit.

c. *Diagnose Option 3.* The software diagnostic program begins with the diagnose option 3 instruction. See figure 4-IIID-5 for the diagnose option 3 instruction format.

The software program may illuminate and extinguish the two DIAGNOSE STATUS lights labeled CPU and IOU. A ONE in bit position 30 will illuminate

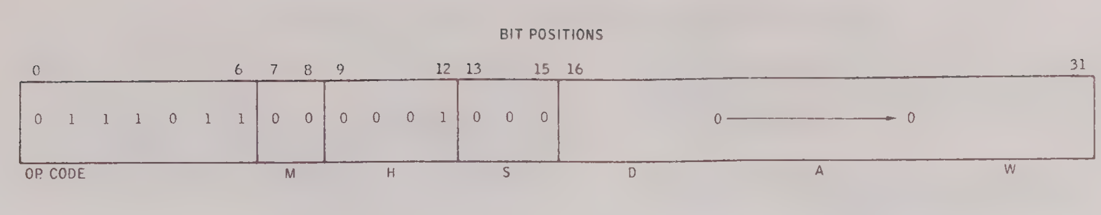
BIT POSITIONS
0
6
7
8
9
12
13
15
16
31
0 1 1 1 0 1 1
0 0
0 0 0 1
0 0 0
0 → 0
OP. CODE
M
H
S
D
A
W
63-1-046

Figure 4-IIID-3. Diagnose Option 1 Instruction Format

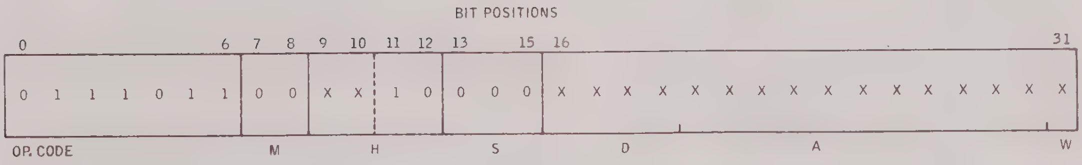
BIT POSITIONS
0
6
7
8
9
10
11
12
13
15
16
31
0 1 1 1 0 1 1
0 0
X X
1 0
0 0 0
X X X X X X X X X X X X X X X X
OP. CODE
M
H
S
D
A
W
63-1-047

Figure 4-IIID-4. Diagnose Option 2 Instruction Format

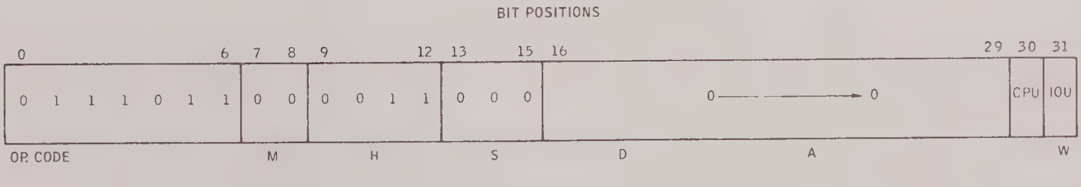
BIT POSITIONS
0
6
7
8
9
12
13
15
16
29
30
31
0 1 1 1 0 1 1
0 0
0 0 1 1
0 0 0
0 → 0
CPU
IOU
OP. CODE
M
H
S
D
A
W
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Figure 4-IIID-5. Diagnose Option 3 Instruction Format

the DIAGNOSE STATUS CPU indicator; a ZERO will extinguish it. A ONE in bit position 31 will illuminate the DIAGNOSE STATUS IOU indicator; a ZERO will extinguish it.

The diagnose option 2 instruction can be used to change the DIAGNOSE CODE as shown in figure 4-IIID-1.

It should be noted that during the software diagnostic the CPU is still in program level 63. As long as the CPU stays in program level 63, the computer is in bootstrap program load which results in the following:

(1) Peripheral devices can be commanded to perform input or output operations.

(2) Peripheral device terminations or interrupts will be accepted; the status bit in the program activity register will be set, but program level changes are inhibited.

(3) Errors will not cause a program level change to program level 2.

Before exit from program level 63, the program should execute an OFR instruction to peripheral device address 02 with bit position 4 in the selected process register being a ONE. This bit will reset the corresponding bit in the monitor register and extinguish the PROGRAM LOAD indicator, PROG LOAD.

When a program in program level 63 executes a call executive program level and link (TXP), or call program level and link (TCP), or tie program level and link (TIE), or test and conditionally reset/skip (TQR) (only when initiating a program level change), or device command and exit (DEX) instruction, then the program level change will take place. Thus, then the bootstrap program load has been completed. Program level changes are permitted and errors will cause a transfer to program level 2.

d. As previously mentioned, pressing the PROGRAM LOAD pushbutton PROG LOAD, will stop the CPU, but not reset it. When bootstrap program load should encounter loading difficulties, it is advisable to master reset the CPU. The procedure includes the following steps:

(1) Press RESTART pushbutton (do not release).

(2) Press PROG LOAD pushbutton (do not release).

(3) Release RESTART pushbutton.

(4) Release PROG LOAD pushbutton.

This procedure will reset the CPU and IOU as well as stopping the CPU before bootstrap program load begins.

Pressing and releasing of the START pushbutton alone will reset the CPU and restart the CPU in program level 1. If there is no program stored in program level 1, then the CPU may encounter error conditions.

Section IV. FRONT PANEL AND MAINTENANCE

This section is subdivided to show the differences in front panels and maintenance that depend upon the application. The subsections to follow are applicable to:

a. TACFIRE

b. AN/TSQ-73

c. AN/TTC-39

d. NICS-TARE

NOTE

The page numbers of the following subsections employ a capital letter reflecting the specific system as indicated above.

4-13A. Front Panel (TACFIRE)

The Central Processing Unit (CPU) and Input Output Unit (IOU) of the computer have the following front panels (computer control console, CCC):

Diagnose Panel (CPU)

Status and Maintenance Panel (IOU)

The Status and Maintenance Panel (IOU) is subdivided into a Status portion and a Maintenance Portion. These panels contain the controls and indicators required by an operator to initialize and monitor system operation. The controls and indicators are arranged in functional groups for rapid identification of individual switch functions.

The Diagnose Panel (CPU) is shown in figure 4-IIIA-2. Table 4-IVA-1 identifies and specifies the functions of the indicator lights located on this panel.

The Status portion of the Status and Maintenance Panel (IOU) is shown in figure 4-IIIA-3, upper part. Table 4-IVA-1 identifies and specifies the functions of the control switches and corresponding indicator lights located on this panel.

NOTE

For convenience, this table has been combined with the table for the Diagnose Panel.

The Maintenance portion of the Status and Maintenance Panel (IOU) is shown in figure 4-IIIA-3, lower part. Table 4-IVA-3 identifies, describes, and specifies the functions of the control switches and corresponding lights located on this panel.

A discussion of the functional operation of the panels is presented in the subsequent paragraphs.

4-14A. Indicators and Controls

Subsequent paragraphs describe the Front Panel indicators and controls.

a. *Setting and Resetting of the Front Panel Control Indicators.* Many of the status and control indicators to be discussed will be programmable. All such indicators have a bit in the monitor register associated with them. In all cases, when the bit in the monitor register is ZERO, the monitor register indicator light is extinguished. However, if the bit in the monitor register is a ONE, the monitor register light remains illuminated. All bits of the monitor register are programmable. The bits of the monitor register (table 4-IVA-4) are set and reset as specified in table 4-IVA-5.

b. *Program Interrogation of the Front Panel.* All controls and corresponding indicator lights on the front panel have either a flip-flop circuit in the monitor register associated with them or they have an inherent storage capability of their own. In either case, all controls and corresponding indicator lights can be interrogated by the computer program using the ITR instruction (refer to table 4-IVA-5).

c. *Front Panel Initiated Interrupts.* The TEST pushbutton, START, on the front panel interrupts the computer (monitor register bit position 5). The interrupt is associated with device address 02. The keyword and termination word associated with device address 02 are located as specified in table 4-IVA-6.

d. *Memory Controls and Indicators.* The 8K core memory banks and the Mass Core Memory Unit (MCMU) banks have the following front panel controls and indicators:

(1) *PWR OFF/OFF-LINE/ON-LINE (rotary switch).* This switch turns the power off to the memory bank. Activation of this switch applies power to the memory bank, and places the memory bank on-line with the CPU/IOU or off-line with the CPU/IOU.

(2) *POWER (green indicator).* Indicates power on in the memory bank.

(3) *POWER FAULT (red indicator).* Indicates power fault in the memory bank power supply.

(4) *OVERTEMP (yellow indicator).* Indicates an excessive temperature detected in the memory bank. Indicator is reset when condition is corrected.

(5) *LAMP TEST (momentary action pushbutton switch).* Applies power to all indicators on the memory bank.

(6) *ADDRESS BANK (two octal thumbwheel switches, 00 to 17).* Select memory bank address to which the memory bank is to respond.

(7) *RUN TIME (meter 0 to 10,000 hours, inside).* Measures elapsed time of memory bank.

4-15A. Monitor Register (TACFIRE)

The monitor register of the Input Output Controller (IOC) contains information pertaining to error conditions detected by the IOC. It also contains information pertaining to bootstrap program load and indicates when the instruction controller has posted a bit in the query register. Table 4-IVA-4 identifies and specifies the functions of each bit in the monitor register.

Input to register (ITR) instruction with peripheral device address 01 can read the monitor register. Output from register (OFR) instruction with peripheral device address 02 selectively resets bits in the monitor register. Output from register (OFR) instruction with peripheral device address 01 selectively sets bits in the monitor register, see table 4-IVA-5.

Table 4-IVA-1. Switch/Indicator Functions on Diagnose Panel and Status Portion of Status and Maintenance Panel (TACFIRE)

DIAGNOSE PANEL - CPU		
Switch/Indicator	Description	Function
POWER	Green indicator	Indicates power on CPU.
LAMP TEST	Momentary action pushbutton switch	Applies power to all indicators on Diagnose Panel.
DIAGNOSE STATUS		
CPU	Amber indicator	Indicates fault detected in CPU (diagnose option 3).
IOU	Amber indicator	Indicates fault detected in IOU (diagnose option 3).
1 to 18	White indicators (18)	Indicate diagnose code or fault number detected during program load or by software (diagnose register bit positions 16 thru 31, 9, and 10; diagnose option 2).
	STATUS PORTION - IOU	
POWER	Alternate action toggle switch	Activation of this switch applies power to the computer (CPU and IOU).
	Green indicator	Indicates power on IOU.
CPU STOPPED	Amber indicator	Indicates when CPU is stopped.
COMPUTER RESTART	Momentary action pushbutton switch, non-illuminated	Activation causes an interrupt to program level 1; similar to restart after power failure.

70061-45-1

Table 4-IVA-1. Switch/Indicator Functions on Diagnose Panel and Status Portion of Status and Maintenance Panel (TACFIRE) (Cont)

STATUS PORTION - IOU		
Switch/Indicator	Description	Function
ALARM RESET	Momentary action pushbutton switch	The setting of monitor register bit positions 1 and 2 sounds an alarm. Pressing the ALARM RESET switch turns the alarm off.
FAULT COMPUTER	Red indicator	Monitor register bit position 2; set by hardware (for conditions, see table 4-IVA-2).
POWER	Red indicator	Indicates fault detected in the computer power supply (CPU or IOU).
SYSTEM	Red indicator	Monitor register bit position 1; set by hardware (for conditions, see table 4-IVA-2).
PROGRAM LOAD CHANNEL 10	Momentary action pushbutton switch with white indicator	Press the pushbutton sets bit position 4 in the monitor register, illuminates indicator, and initiates a program load from peripheral device address 10. Program resets this bit position.
CHANNEL 11	Momentary action pushbutton switch with white indicator	Press the pushbutton sets bit position 3 in the monitor register, illuminates a program load from peripheral device address 11. Program resets this bit position.

70061-45-2A

Table 4-IVA-1. Switch/Indicator Functions on Diagnose Panel and Status Portion of Status and Maintenance Panel (TACFIRE) (Cont)

STATUS PORTION - IOU		
Switch/Indicator	Description	Function
COMPUTER INTERRUPT	Momentary action pushbutton switch with white indicator	Pressing the pushbutton sets bit position 0 in the monitor register, illuminates indicator, and interrupts the computer from peripheral device address 02. Program resets this bit position.
TEST		
XX	Two octal thumbwheel switches (00 to 77)	Indicate test number (maintenance register bit positions 16 to 21).
START	Momentary action pushbutton switch with white indicator.	Pressing the pushbutton sets bit position 5 in the monitor register, illuminates indicator, and interrupts the computer using peripheral device address 02. Program resets this bit position.
LAMP TEST	Momentary action pushbutton switch.	Applies power to all indicators on the IOU (Status and Maintenance Panel).

70061-45-3

Table 4-IVA-2. Monitor Register Error Conditions for Bit Positions 1 and 2 (TACFIRE)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set		
			Monitor Register	Query Register	Indicator Register
1 and 2	Device response time out - 10 microseconds (device hung up; set by IOC)	Yes	9		
1 and 2	I/O memory parity error on control word (set by IOC)	Yes	11		
1 and 2	I/O memory parity error on data word (set by IOC)	Yes	12		
1 and 2	Memory time out - 60 microseconds (set by IOC)	Yes	13		
1 and 2	IOC time out - 260 microseconds (IOC failed to honor real time clock request)	Yes	14		
1 and 2	Program time out - 1024 microseconds (set by IOC real-time clock zero not initiatized, or Mode 0 in keyword)	Yes	15		
2 only	Input on output error (set by IOC)	Yes	7		
2 only	I/O memory access violation (set by IOC)	Yes	10		
2 only	Instruction parity error (set by CPU)	Yes		0	
2 only	Level change parity error (set by CPU)	Yes		1	
2 only	Instruction violation (set by CPU)	Yes		2	
2 only	Memory access violation (set by CPU)	Yes		3	

NOTE 1: Bit Position, 1 System Fault
Bit Position, 2 Computer Fault

70061-46-1

Table 4-IVA-2. Monitor Register Error Conditions for Bit Positions 1 and 2 (TACFIRE) (Cont)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set		
			Monitor Register	Query Register	Indicator Register
2 only	Memory time out (set by CPU)	Yes		4	
2 only	Specification violation (set by CPU)	Yes		5	

NOTE 1: Bit Position, 1 System Fault
Bit Position, 2 Computer Fault

70061-46-2

The setting of specific bits in the monitor register (table 4-IVA-4) causes a program interrupt. The interrupt uses peripheral device address 02 termination word to stimulate a program level. The memory locations for the keyword and termination word for peripheral device address 02 are shown in table 4-11A.

Table 4-IVA-4 also lists the monitor register bit positions which are displayed on the front panel and being affected by front panel pushbuttons; see also description of Front Panel (figures 4-III-2 and 4-IIIA-3 and tables 4-IVA-1 and 4-IVA-3).

Subsequent paragraphs describe the functions of the bit positions in the monitor register:

a. *Computer Interrupts Bit Position 0.* Pressing a pushbutton causes a computer interrupt using peripheral device address 02.

b. *System Fault, Bit Position 1.* This bit is set as a result of the setting of bits in the monitor register, as shown in table 4-IVA-2.

c. *Computer Fault, Bit Position 2.* This bit position is set as a result of the setting of bits in the monitor register and query register, as shown in table 4-IVA-2.

d. *Program Load Channel 11, Bit Position 3.* This bit is set when the PROGRAM LOAD button, CHANNEL 11, is pressed.

e. *Program Load Channel 10, Bit Position 4.* This bit is set when the PROGRAM LOAD button, CHANNEL 10, is pressed.

f. *Start, Bit Position 5.* This bit is set when the TEST button, START, is pressed. It causes a computer interrupt using peripheral device address 02. The test to be performed can be specified by the two test thumbwheels. The thumbwheels are connected to the maintenance register, which can be read by an ITR instruction with peripheral device address 02.

g. *Not Used, Bit Position 6.* This bit position is used only in AN/TSQ-73. It indicates a secondary CPU fault.

h. *Input on Output Error, Bit Position 7.* This bit is set when a peripheral device inputs data while the keyword specifies output, modes 1, 4, and 5.

i. *Device Input Parity Error, Bit Position 8.* This bit is set when an input parity error occurs during bootstrap program load (IOC will be stopped).

This bit is also set when an input parity error is detected during automatic input and the P-bit in the termination word is a ONE. The program level (EPL) as specified in the termination word will be stimulated (not program level 2, unless EPL = 2).

j. *Device Time Out, Bit Position 9.* This bit is set when a peripheral device time out occurs during an I/O operation (peripheral device hang up). This bit is set when a peripheral device is not responding to the IOC's address/enable sequence within 10 microseconds in the automatic input mode.

An automatic transfer to program level 2 is also initiated.

k. *I/O Memory Access Violation, Bit Position 10.* This bit is set when a memory access violation occurs during an input or output operation.

Table 4-IVA-3. Switch/Indicator Functions on Maintenance Portion of Status and Maintenance Panel (TACFIRE)

Switch/Indicator	Description	Function
DATA EXCHANGE CHANNEL	White indicators (3)	Indicate most significant octal digit of peripheral device address when an I/O error has been detected (monitor register bit positions 26 to 28).
DEVICE CHANNEL	White indicators (3)	Indicate least significant octal digit of peripheral device address when an I/O error has been detected (monitor register bit positions 29 to 31).
I/O CHANNEL FAULT CONTINUITY	Amber indicator	Indicates when I/O cable is not connected or not terminated (maintenance register bit position 15).
PARITY	Amber indicator	Indicates peripheral device input parity error; set by IOC (monitor register bit position 8).
TIME OUT	Amber indicator	Indicates peripheral device failed to respond to the IOC within 10 microseconds (monitor register bit position 9).
MEMORY CHANNEL	White indicators (3)	Indicate memory bank address when IOC detects a memory parity error, access violation, or time-out occurs (monitor register bit positions 22 to 24).
MEMORY FAULT CONTINUITY	Amber indicator	Indicates when memory cable is not connected or not terminated (maintenance register bit position 15).

70061-47-1A

Table 4-IVA-3. Switch/Indicator Functions on Maintenance Portion of Status and Maintenance Panel (TACFIRE) (Cont)

Switch/Indicator	Description	Function
MEMORY FAULT PARITY	Amber indicator	Indicates a detected memory parity error by the CPU (query register bit positions (0 or 1) or by the IOU (monitor register bit positions 11 or 12).
TIMEOUT	Amber indicator	Indicates a detected memory time-out by the CPU (query register bit position 4) or by the IOU (monitor register bit position 13).
TIMEOUT FAULT IOC	Amber indicator	Indicates the IOU failed to honor a real-time clock request in 256 microseconds (monitor register bit position 14).
PROGRAM	Amber indicator	Indicates program failed to initialize keyword for real-time clock 0 in 1024 microseconds or when Mode 0 in keyword is encountered (monitor register bit position 15).
ACC ADDRESS	Two octal thumbwheel switches (00 to 77)	Indicate peripheral device address for Artillery Control Console (maintenance register bit positions 26 to 31).
DATA EXCHANGE CHANNEL SELECT A/B/C	Three-position rotary switches (3)	Determine data exchange number 1 to 7, or off-line, of IOX A/B/C; this number corresponds to most significant octal digit of peripheral device address for I/O cable A/B/C.

70061-47-2A

Table 4-IVA-4. Monitor Register Bit Identification and Bit Functions (TACFIRE)

Bit Positions	Notes	C[1]	I[2]	L[3]	Function
00	4, 5		X		Computer interrupt
01	6		X	X	System fault
02	6		X	X	Computer fault
03	4, 7		X		Program load channel 11
04			X		Program load channel 12
05	5		X		Start (program test)
06	7				Not used (secondary CPU fault)
07					Input on output error (set by IOC)
08			X		Device input parity error (set by IOC)
09			X	X	Device time out - 10 microseconds (peripheral device hung up, set by IOC)
10				X	I/O memory access violation (set by IOC)
11	8		X	X	I/O memory parity error on control word (set by IOC)
12	8		X	X	I/O memory parity error on data word (set by IOC)
13			X	X	Memory time out - 60 microseconds (set by IOC)

[1] C = CPU

[2] I = IOU

[3] L = Stimulates program level 2

[4] Used in TACFIRE

[5] Pressing these buttons causes an interrupt

[6] See table 4-IVA-2 for all conditions that set these bits

[7] Used in AN/TSQ-73

[8] ORed, one indicator; also, ORed with query register bit positions 0 and 1

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Table 4-IVA-4. Monitor Register Bit Identification and Bit Functions (TACFIRE) (Cont)

Bit Positions	Notes	C[1]	I[2]	L[3]	Function
14			X	X	IOC time out - 256 microseconds (IOC failed to honor real-time clock request)
15			X	X	Program time out - 1024 microseconds (set by IOC, real-time clock zero not initialized, or Mode 0 in keyword)
16					I/O avalanche error (multiple I/O errors)
17-20					MCMU bank address (for I/O data transfers only, keywords and termination words remain in base memory bank)
21-24			X		Memory bank address when IOC detects a memory parity error, access violation occurs, or time out (bit 21 is ZERO, bit 22 is MSB of memory address)
25-31					Device address (when any peripheral device error occurs, bit 25 is ZERO, bit 26 is MSB of peripheral device address) DATA EXCHANGE CHANNEL/DEVICE CHANNEL

[1] C = CPU

[2] I = IOU

[3] L = Stimulates program level 2

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Table 4-IVA-5. Monitor/Maintenance Registers, Read or Modify

*Computer Instruction	Device Address (01)	Device Address (02)
OFR	Sets bits in the monitor register A ONE in bit position N of (H) sets a one in the corresponding bit position of the monitor register	Resets bits in the monitor register A ONE in bit position N of (H) resets to ZERO to corresponding bit of the monitor register
ITR	Reads monitor register into specified process register	Reads maintenance register into specified process register

*Example of OFR instruction: Assume the following OFR instruction is executed.

BIT POSITIONS

0	1 6	7 8	9 12	13 15	16 31
0	OFR	0 0	0100	000	000002
E	F	M	H	S	D A W

This instruction will cause bit position 10 of the monitor register to be reset when bit position 10 in process register 4 (H = 0100) is a ONE.

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Table 4-IVA-6. Keyword and Termination Word for Device Address 02

	Base Memory Location	
Device Address	Key Word	Termination Word
02	78_{16}	$7A_{16}$

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An automatic transfer to program level 2 is also initiated. There is no indicator on the front panel.

l. *I/O Memory Parity Error on Control Word, Bit Position 11.* This bit is set when the IOC detects a memory parity error when accessing the base memory bank (keyword, termination word, program activity register, queue register).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 12 for display on the front panel.

m. *I/O Memory Parity Error on Data Word, Bit Position 12.* This bit is set when the IOC detects a memory parity error when accessing memory for data transfers (full word output, byte output, byte input).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 11 for display on the front panel.

n. *Memory Time Out, Bit Position 13.* This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request by the IOC.

An automatic transfer to program level 2 is also initiated.

o. *IOC Time Out, Bit Position 14.* This bit is set when the IOC fails to honor a real-time clock request (any of the three) within 256 microseconds.

An automatic transfer to program level 2 is also initiated.

p. *Program Time Out, Bit Position 15.* This bit is set when the IOC detects that the keyword-block, length field for the real-time clock zero (peripheral device address 03) is zero. The program should have reinitialized this field within 1,024 microseconds after it has been decremented to zero.

An automatic transfer to program level 2 is also initiated.

q. *I/O Avalanche Error, Bit Position 16.* The setting of any bit positions 7, 9 through 15 indicates that an error has occurred that stimulated program level 2. The setting of any one of these bit positions will set a flip-flop (not related to bit position 16) inhibiting any further setting until an OFR instruction to peripheral device address 01 or 02 has been executed. This OFR instruction will enable the setting of bit positions 7, 9 through 15 in the monitor register; the OFR instruction is effective even when all bits in the selected process register are all zeros. The avalanche error, bit position 16, will be set when the IOC detects a second I/O related error before a first error, which stimulated program level 2, has been cleared by executing an OFR instruction to peripheral address 01 or 02.

r. *MCMU Bank Address, Bit Positions 17 through 20.* This 4-bit field specifies the Mass Core Memory Unit (MCMU) bank address to be used for I/O data transfers.

NOTE

The keywords and termination words remain in the base memory bank.

s. *Memory Bank Address, Bit Positions 21 through 24.* Bit position 21 is ZERO; bit position 22 is the most significant bit of the memory address. These bits are set when the IOC detects one of the following conditions:

(1) Memory parity error.
(2) Memory access violation.
(3) Memory time out.
(4) No update on second error.

t. *Device Address, Bit Positions 25 through 31.* Bit position 25 is ZERO; bit position 26 is the most significant bit of the peripheral device address. These bits are set when the IOC detects an error, which cause to set any bit positions 9 through 15.

NOTE

The device address bits are also set under two conditions that do not stimulate program level 2. First, when an input parity error is detected during bootstrap program load, monitor register bit 8 will be set and the IOC stops. Second, when an input parity error is detected during an automatic input and the P-bit in the termination word is a ONE. The program level (EPL), as specified in the termination word, will be stimulated (not program level 2, unless EPL = 2); the device address may be ambiguous for this second case.

4-16A. Maintenance Register (TACFIRE)

The maintenance register is an extension of the monitor register. This register uses only control inputs from switches or control lines. Thus, the register can be read by the computer but bits cannot be reset. Bits are changed by changing thumbwheel switches and control lines.

Table 4-IVA-7 lists the bit positions and functions assigned to the maintenance register. The maintenance register can be read by the computer using an ITR instruction with peripheral device address 02.

4-17A. Special Input/Output (I/O) Addresses (TACFIRE)

Table 4-IVA-8 lists the functions of the special I/O addresses listed in table 4-2.

Table 4-IVA-7. Maintenance Register (TACFIRE) (Read with ITR Instruction, Device Address 02)

Bit Positions	Indicator	Remarks
0-14	Not used[1]	
15	CONTINUITY[2]	Bit = 0 when all I/O and memory cables are connected and terminated.
16-21	TEST thumbwheel[2] (PROGRAM TEST)[3, 4]	Bit positions 16 to 18 associated with most significant thumbwheel, bit positions 19 to 21 associated with least significant thumbwheel (64 selections).
22-24	None[2]	Define memory bank to be base memory.
25-31	ACC ADDRESS [2]	Indicate to which peripheral device address the Artillery Control Console is connected (bit position 25 is ZERO, bit positions 26 to 28 are associated with most significant thumbwheel and bit positions 29 to 31 are associated with least significant thumbwheel.
27	(None)[4]	(Processor 1/2)[4]
29-31	(PROGRAM LOAD rotary device select)[3, 4]	(Peripheral device address)[3, 4]

[1] Used in AN/TSQ-73

[2] Used in TACFIRE

[3] Used in AN/TTC-39

[4] Used in NICS-TARE

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Table 4-IVA-8. Special I/O Device Address Functions

Device Address	Function
00	Interrupt, and start secondary CPU are controlled by operand bit positions 0 and 1 respectively[1]. The OFR instruction with peripheral device address 00 is used to set the memory access control bits for input/output. The OFR instruction is further defined in table 4-5.
01	Device address 02 has two instructions associated with it. An ITR instruction with peripheral device address 01 reads the monitor register. An OFR instruction with peripheral device address 01 sets flip-flops in the monitor register.
02	Using an OFR instruction with peripheral device address 02 allows the monitor register to be reset. Using an ITR instruction with peripheral device address 02 allows the maintenance register to be read. The status panel interrupt occurs on peripheral device address 02. The keyword should be all zeros for peripheral device address 02.
03	Device address applies to real-time clock zero. A device command with peripheral device address 03 will allow the program to turn on or off real-time clock zero, as well as real-time clocks one and two. The format for the DEV instruction for control of the real-time clocks is shown in figure 4-6. All three real-time clocks are controlled by sending the command to peripheral device address 03. The keyword for peripheral device addresses 04 and 05 should use the alarm mode (mode 2).
04 and 05	Device addresses 04 and 05 are associated with real-time clocks one and two respectively. The format for the DEV instruction for control of the real-time clocks is shown in figure 4-6.
06 and 07	Device addresses 06 and 07 are associated with CSIN (COMSEC)[2]

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[1] Used in AN/TSQ-73

[2] Used in TACFIRE

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Section IVB. FRONT PANEL AND MAINTENANCE (AN/TSQ-73)

4-13B. ADP Status and Control Panel (AN/TSQ-73)

The AN/TSQ-73 has one front panel called the Automatic Data Processor (ADP) Status and Control Panel. It consist of:

a. Status portion

b. Control portion

The ADP Status and Control Panel of the computer contains the controls and indicators required by an operator to initialize and monitor system operation. The controls and indicators are arranged in functional groups for rapid identification of individual switch functions.

The Status portion of the ADP Status and Control Panel is shown in figure 4-IIIB-2. Table 4-IVB-1 identifies and specifies the functions of the control switches and corresponding indicator lights located on the Status portion of the ADP Status and Control Panel.

The Control portion of the ADP Status and Control Panel is shown in figure 4-IVB-1. Table 4-IVB-2 identifies, describes, and specifies the functions of the control switches and corresponding lights located on the Control portion of the ADP Status and Control Panel.

A discussion of the functional operation of the ADP Status and Control Panel is presented in the subsequent paragraphs.

4-14B. Indicators and Controls (AN/TSQ-73)

a. *Setting and Resetting of the ADP Status and Control Panel Control Indicators.* Many of the status and control indicators to be discussed will be programmable. All such indicators have a bit in the monitor register associated with them. In all cases, when the bit in the monitor register is ZERO, the monitor register indicator light is extinguished. However, if the bit in the monitor register is a ONE, the monitor register light remains illuminated. All bits of the monitor register are programmable. The bits of the monitor register (table 4-IVB-3) are set and reset as specified in table 4-IVA-5.

b. *Program Interrogation of the ADP Status and Control Panel.* All controls and corresponding indicator lights on the ADP Status and Control Panel have either a flip-flop circuit in the monitor register associated with them or they have an inherent storage capability of their own. In either case, all controls and corresponding indicator lights can be interrogated by the computer program using the ITR instruction (refer to table 4-IVA-5).

c. *ADP Status and Control Panel Initiated Interrupts.* The program test pushbutton, START, on the ADP Status and Control Panel interrupts the computer (monitor register bit position 5). The interrupt is associated with device address 02. The keyword and termination word associated with device address 02 are located as specified in table 4-IVA-6.

4-15B. Monitor Register (AN/TSQ-73)

The monitor register of the input output controller (IOC) contains information pertaining to error conditions detected by the IOC. It also contains information pertaining to bootstrap program load and indicates when the instruction controller has posted a bit in the query register. Table 4-IVB-3 identifies and specifies the functions of each bit in the monitor register.

Input to register (ITR) instruction with peripheral device address 01 can read the monitor register. Output from register (OFR) instruction with peripheral device address 02 selectively resets bits in the monitor register. Output from register (OFR) instruction with peripheral device address 01 selectively sets bits in the monitor register, see table 4-IVA-5.

The setting of specific bits in the monitor register (table 4-IVB-3) causes a program interrupt. The interrupt uses peripheral device address 02 termination word to stimulate a program level. The memory locations for the keyword and termination word for peripheral device address 02 are shown in table 4-11A.

Table 4-IVB-3 also lists the monitor register bit positions which are displayed on the front panel and being affected by front panel pushbuttons; see also description of ADP Status and Control Panel (figures 4-IIIB-2 and 4-IVB-1 and tables 4-IVB-1 and 4-IVB-2).

Subsequent paragraphs describe the functions of the bit positions in the monitor register:

a. *Not Used, Bit Position 0.* This bit position is used only in TACFIRE. Pressing a pushbutton causes a computer interrupt using peripheral device address 02.

b. *IOU Fault, Bit Position 1.* This bit is set as a result of the setting of bits in the monitor register, as shown in table 4-IVB-4.

c. *Primary CPU Fault, Bit Position 2.* This bit position is set as a result of the setting of bits in the monitor register and query register by the primary CPU as shown in table 4-IVB-4.

d. *Program Load Channel 11, Bit Position 3.* This bit is set when the PROGRAM LOAD button, CHAN 11, is pressed.

e. *Program Load Channel 10, Bit Position 4.* This bit is set when the PROGRAM LOAD button, CHAN 10, is pressed.

Table 4-IVB-1. Switch/Indicator Functions on Status Portion of ADP Status and Control Panel (AN/TSQ-73)

Switch/Indicator	Description	Function
UPPER CPU DIAGNOSE STATUS IOU/CPU	Amber indicators (2)	Indicate fault detected in IOU (if primary CPU) or CPU (diagnose option 3).
DIAGNOSE CODE	Six octal digits, light emitting diodes	Indicate diagnose code or fault number detected during program load or by software (diagnose register bit positions 16 through 31, 9, and 10; diagnose option 2).
PROG LOAD STATUS IOU/CPU	Amber indicators (2)	Indicate a fault in the IOU (if primary CPU) or CPU during program load.
LOWER CPU	Same as upper CPU	Same as upper CPU
PRIMARY CPU RUN/INHIBIT	Two-position toggle switch (guarded)	RUN position allows CPU to automatically start. INHIBIT position prevents CPU from running until switch is moved to RUN position.
STOPPED	Red indicator	Indicates when CPU is stopped.
RESTART	Momentary action pushbutton switch, non-illuminated white switch cap	Activation causes an interrupt to program level 1; similar to restart after power failure.
PROGRAM LOAD CHAN 10	Momentary action pushbutton switch (guarded)with white indicator (Channel 10)	Pressing the pushbutton sets bit position 4 in the monitor register, illuminates indicator, and initiates a program load from peripheral device 10. Program resets this bit portion.

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Table 4-IVB-1. Switch/Indicator Functions on Status Portion of ADP Status and Control Panel (AN/TSQ-73) (Cont)

Switch/Indicator	Description	Function
PRIMARY CPU (Cont) PROGRAM LOAD (Cont) CHAN 11	Momentary action pushbutton switch (guarded) with white indicator (Channel 11)	Pressing the pushbutton sets bit position 3 in the monitor register, illuminates indicator, and initiates a program load from peripheral device 11. Program resets this bit position.
FAULT PRIME CPU	Amber indicator (Primary CPU)	Monitor register bit position 2; set by hardware, primary CPU (for conditions, see Table 4-9B).
SEC CPU	Amber indicator (Secondary CPU)	Monitor register bit position 6; set by hardware, secondary CPU (for conditions, see Table 4-9B).
IOU	Amber indicator	Monitor register bit position 1; set by hardware, IOU (for conditions, see Table 4-9B).
TIME OUT IOU/ PROG	Amber indicators (2) (Program)	Indicate the IOU failed to honor a real-time clock request in 256 microseconds (monitor register bit position 14) and program failed to initialize keyword for real-time clock 0 in 1024 microseconds or when Mode 0 in keyword is encountered (monitor register bit position 15).

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Table 4-IVB-1. Switch/Indicator Functions on Status Portion of ADP Status and Control Panel (AN/TSQ-73) (Cont)

Switch/Indicator	Description	Function
FAULT (Cont) DEVICE ERROR PARITY/ T-OUT	Amber indicators (2) (Time-Out)	Indicate peripheral device input parity error, set by IOC (monitor register bit position 8) and peripheral device failed to respond to the IOC within 10 microseconds (monitor register bit position 9).
DEVICE ADDRESS	Two octal digits, light emitting diodes	Indicate peripheral device address when an I/O error has been detected (monitor register bit portions 26 to 31).
MEMORY ERROR PARITY IOU/ CPU	Amber indicators (2)	*Indicate a detected memory parity error by the IOU (monitor register bit position 11 or 12) or by the CPU (query register bit position 0 or 1).
MEMORY ERROR TIME OUT IOU/ CPU	Amber indicators (2)	*Indicate a detected memory time out by the IOU (monitor register bit position 13) or by the CPU (query register bit position 13). *Fault conditions are set by either CPU (upper or lower). PRIME or SEC CPU will also illuminate to indicate which CPU caused the fault.

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Table 4-IVB-1. Switch/Indicator Functions on Status Portion of ADP Status and Control Panel (AN/TSQ-73) (Cont)

Switch/Indicator	Description	Function
FAULT (Cont) MEMORY ERROR (Cont) IOU MEM BANK	One octal digit, light emitting diodes	Indicates memory bank address when IOC detects a memory parity error, access violation, or time out (monitor register bit positions 22 to 24).
SECONDARY CPU RUN/INHIBIT STOPPED RESTART	Same as primary CPU	Same as primary CPU
START	Momentary action pushbutton switch with white indicator	To be used after completion of bootstrap program load to start secondary CPU. IOU enables this switch after successful completion of bootstrap program load.

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f. *Start, Bit Position 5.* This bit is set when the PROGRAM TEST button, START, is pressed. It causes a computer interrupt using peripheral device address 02. The test to be performed can be specified by the two program test thumbwheels. The thumbwheels are connected to the maintenance register which can be read by an ITR instruction with peripheral device address 02.

g. *Secondary CPU Fault, Bit Position 6.* This bit position is set as a result of the setting of bits in the query register, by the secondary CPU, as shown in table 4-IVB-4.

h. *Input on Output Error, Bit Position 7.* This bit is set when a peripheral device inputs data while the keyword specifies output, modes 1, 4, and 5.

i. *Device Input Parity Error, Bit Position 8.* This bit is set when an input parity error occurs during bootstrap program load (IOC will be stopped).

This bit is also set when an input parity error is detected during automatic input and the P-bit in the termination word is a ONE. The program level (EPL) as specified in the termination word will be stimulated (not program level 2, unless EPL = 2).

j. *Device Time Out, Bit Position 9.* This bit is set when a peripheral device time out occurs during an I/O operation (peripheral device hang up). This bit is set when a peripheral device is not responding to the IOC's address/enable sequence within 10 microseconds in the automatic input mode.

An automatic transfer to program level 2 is also initiated.

k. *I/O Memory Access Violation, Bit Position 10.* This bit is set when a memory access violation occurs during an input or output operation.

An automatic transfer to program level 2 is also initiated. There is no indicator on the front panel.

l. *I/O Memory Parity Error on Control Word, Bit Position 11.* This bit is set when the IOC detects a memory parity error when accessing the base memory bank (keyword, termination word, program activity register, queue register).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 12 for display on the front panel.

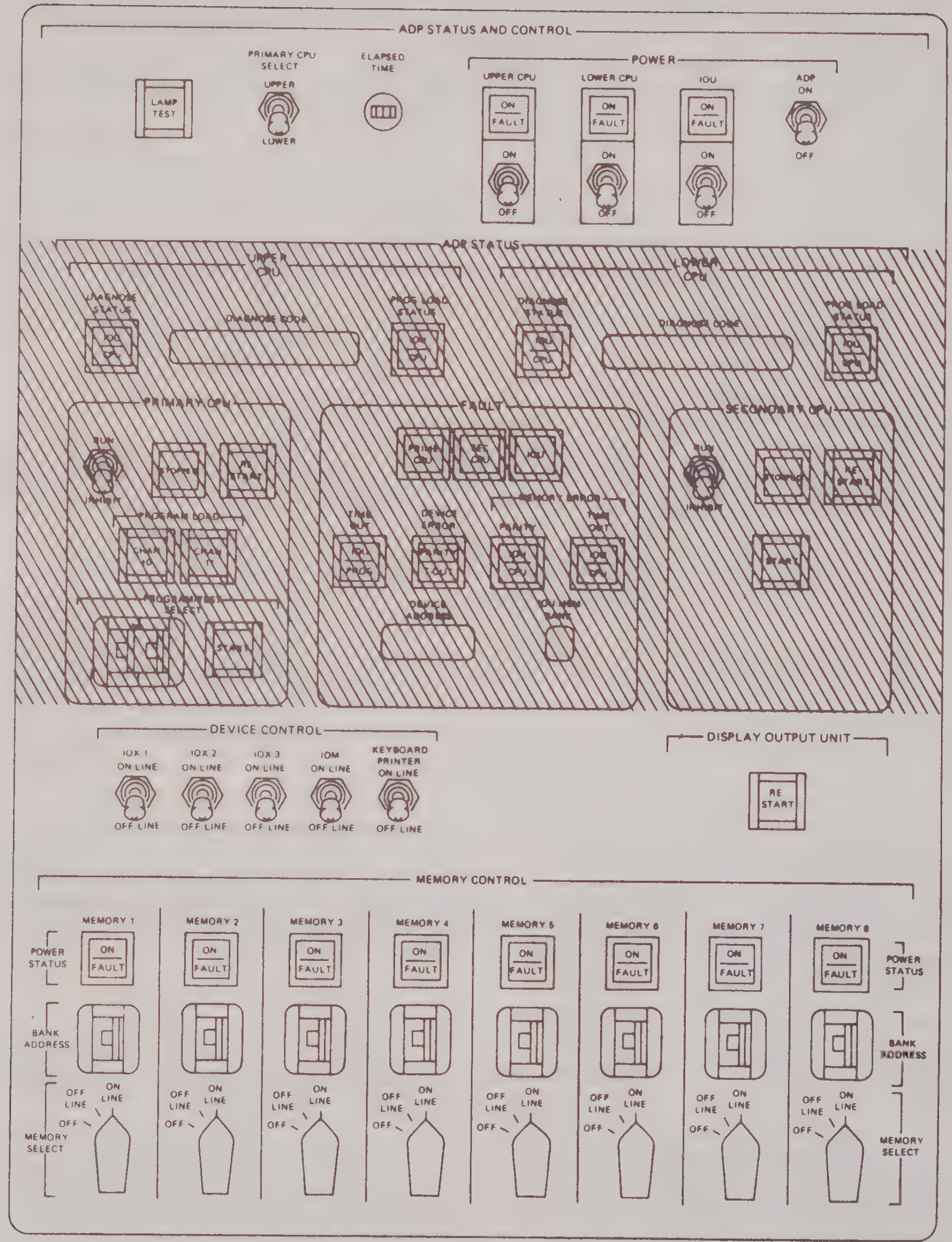
ADP STATUS AND CONTROL
LAMP TEST
PRIMARY CPU SELECT
UPPER
LOWER
ELAPSED TIME
POWER
UPPER CPU
LOWER CPU
IOU
ON
FAULT
ON
OFF
ADP ON
OFF
ADP STATUS
UPPER CPU
LOWER CPU
DIAGNOSE STATUS
DIAGNOSE CODE
PROG LOAD STATUS
IOU
CPU
PRIMARY CPU
FAULT
SECONDARY CPU
RUN
INHIBIT
STOPPED
RE START
PROGRAM LOAD
CHAN 10
CHAN 11
PROGRAM/TEST SELECT
START
PRIME CPU
SEC CPU
IOU
MEMORY ERROR
TIME OUT
DEVICE ERROR
PARITY
TIME OUT
IOU
PROG
PARITY
T-OUT
DEVICE ADDRESS
DEVICE CONTROL
IOX 1 ON LINE
IOX 2 ON LINE
IOX 3 ON LINE
IOM ON LINE
KEYBOARD PRINTER ON LINE
OFF LINE
DISPLAY OUTPUT UNIT
RE START
MEMORY CONTROL
MEMORY 1
MEMORY 2
MEMORY 3
MEMORY 4
MEMORY 5
MEMORY 6
MEMORY 7
MEMORY 8
POWER STATUS
ON
FAULT
BANK ADDRESS
OFF LINE
ON LINE
OFF
MEMORY SELECT
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Figure 4-IVB-1. Control Portion of ADP Status and Control Panel

Table 4-IVB-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (AN/TSQ-73)

Switch/Indicator	Description	Function
LAMP TEST	Momentary action pushbutton switch	Applies power to all indicators on ADP Status and Control Panel.
PRIMARY CPU SELECT UPPER/LOWER	Two-position toggle switch (guarded)	Selects upper or lower CPU to be designated as primary CPU.*
ELAPSED TIME	Meter	Measures elapsed time on IOU.
POWER UPPER CPU ON/FAULT	Green/red indicators (2) (upper CPU)	Indicate power on upper CPU/power fault in upper CPU power supply.
ON/OFF	Two-position toggle switch	Power switch to upper CPU.
LOWER CPU ON/FAULT	Green/red indicators (2)	Indicate power on lower CPU/power fault in lower CPU power supply.
ON/OFF	Two-position toggle switch	Power switch to lower CPU.
IOU ON/FAULT	Green/red indicators (2) (IOU)	Indicate power on IOU/ power fault in IOU power supply.
ON/OFF	Two-position toggle switch	Power switch to IOU.

*Indicator register of individual CPU (bit position 5); ZERO = primary CPU, and ONE = secondary CPU.

Maintenance register (bit position 6); ZERO = lower CPU as primary CPU, and ONE = upper CPU as primary CPU.

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Table 4-IVB-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (AN/TSQ-73) (Cont)

Switch/Indicator	Description	Function
POWER (Cont) ADP ON/OFF	Two-position toggle switch (guarded)	Power switch to all ADP equipment.
PROGRAM TEST XX	Two octal thumbwheel switches (00 to 77)	Indicate program test number (maintenance register bit positions 16 to 21).
START	Momentary action pushbutton with white indicator	Pressing of the pushbutton sets bit position 5 in the monitor register, illuminates indicator, and interrupts the computer using peripheral device address 02. Program resets this bit position.
DEVICE CONTROL IOX 1 ON LINE/ OFF LINE	Two-position toggle switch (guarded) (Input Output Exchange 1)	Places IOX 1 on-line or off-line. In OFF LINE, peripheral devices connected to IOX 1 cannot communicate with computer. (Maintenance register bit position 10).
IOX 2 IOX 3 IOM KEYBOARD PRINTER	(Input Output Multiplexer) (KPU)	Same as IOX 1 Maintenance register bit position 11 to 14).
DISPLAY OUTPUT UNIT Restart	Momentary action pushbutton switch with white indicator	When pressed, this switch causes the DOU to fetch the control word from address zero to start the output operation.

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Table 4-IVB-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (AN/TSQ-73) (Cont)

Switch/Indicator	Description	Function
MEMORY CONTROL POWER STATUS ON/FAULT	Green/red indicators (2)	Indicate power on memory bank/power fault in memory power supply.
BANK ADDRESS X	One octal thumbwheel switch (0 to 7)	Selects memory bank address to which memory bank is to respond.

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m. *I/O Memory Parity Error on Data Word, Bit Position 12.* This bit is set when the IOC detects a memory parity error when accessing memory for data transfers (full word output, byte output, byte input).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 11 for display on the front panel.

n. *Memory Time Out, Bit Position 13.* This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request by the IOC.

An automatic transfer to program level 2 is also initiated.

o. *IOC Time Out, Bit Position 14.* This bit is set when the IOC fails to honor a real-time clock request (any of the three) within 256 microseconds.

An automatic transfer to program level 2 is also initiated.

p. *Program Time Out, Bit Position 15.* This bit is set when the IOC detects that the keyword block length field for the real-time clock zero (peripheral device address 03) is zero. The program should have reinitialized this field within 1,024 microseconds after it has been decremented to zero.

An automatic transfer to program level 2 is also initiated.

q. *Not Used, Bit Position 16.* This bit position is used in TACFIRE, AN/TTC-39, and NICS-TARE to indicate an I/O Avalanche Error. The setting of any bit positions 7, 9 through 15 indicates that an error has occurred that stimulated program level 2. The setting of any one of these bit positions will set a flip-flop (not related to bit position 16) inhibiting any further setting until an OFR instruction to peripheral device address 01 or 02 has been executed. This OFR instruction will enable the setting of bit positions 7, 9 through 15 in the monitor register; the OFR instruction is effective even when all bits in the selected process register are all zeros. The avalanche error, bit position 16 will be set when the IOC detects a second I/O related error before a first error, which stimulated program level 2, has been cleared by executing an OFR instruction to peripheral address 01 or 02.

r. *Not Used, Bit Positions 17 through 20.* This 4-bit field specifies the Mass Core Memory Unit (MCMU) bank address to be used for I/O data transfers in TACFIRE, AN/TTC-39, and NICS-TARE.

NOTE

The keywords and termination words remain in the base memory bank.

s. *Not Used, Bit Positions 21 through 24.* These bit positions are used in TACFIRE, AN/TTC-39, and NICS-TARE to indicate the Memory Bank Address. Bit position 21 is ZERO, bit position 22 is the most significant bit of the memory address. These bits are set when the IOC detects one of the following conditions:

(1) Memory parity error.

(2) Memory access violation.

(3) Memory time out.

(4) No update on second error.

t. *Device Address, Bit Positions 25 through 31.* position 25 is the most significant bit of the peripheral device address. These bits are set when the IOC detects an error which cause to set any bit positions 9 through 15.

NOTE

> The device address bits are also set under two conditions that do not stimulate program level 2. First, when an input parity error is detected during bootstrap program load, monitor register bit 8 will be set and the IOC stops. Second, when an input parity error is detected during an automatic input and the P-bit in the termination word is a ONE. The program level (EPL), as specified in the termination word, will be stimulated (not program level 2, unless EPL = 2); the device address may be ambiguous for this second case.

4-16B. Maintenance Register (AN/TSQ-73)

The maintenance register is an extension of the monitor register. This register uses only control inputs from switches or control lines. Thus, the register can be read by the computer but bits cannot be reset. Bits are changed by changing thumbwheel switches and control lines.

Table 4-IVB-5 lists the bit positions and functions assigned to the maintenance register. The maintenance register can be read by the computer using an ITR instruction with peripheral device address 02.

4-17B. Special Input/Output (I/O) Addresses (AN/TSQ-73)

Table 4-IVA-8 lists the functions of the special I/O addresses listed in table 4-2.

Table 4-IVB-3. Monitor Register Bit Identification and Bit Functions (AN/TSQ-73)

Bit Positions	Notes	S[1]	C[2]	L[3]	Function
00	4,5				Not used (computer interrupt)
01	6			X	IOU fault (system fault)
02	6			X	Primary CPU fault (computer fault)
03	4,7				Program load channel 11
04		X			Program load channel 12
05	5		X		Start (program test)
06	7				Secondary CPU fault
07					Input on output error (set by IOC)
08		X			Device input parity error (set by IOC)
09		X		X	Device time out - 10 microseconds (peripheral device hung up, set by IOC)
10				X	I/O memory access violation (set by IOC)
11	8	X		X	I/O memory parity error on control word (set by IOC)
12	8	X		X	I/O memory parity error on data word (set by IOC)
13		X		X	Memory time out - 60 microseconds (set by IOC)

[1] S = Status portion of ADP Status and Control Panel

[2] C = Control portion of ADP Status and Control Panel

[3] L = Stimulates program level 2

[4] Used in TACFIRE

[5] Pressing these buttons causes an interrupt

[6] See table 4-IVB-4 for all conditions that set these bits

[7] Used in AN/TSQ-73

[8] ORed, one indicator; also, ORed with query register bit positions 0 and 1

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Table 4-IVB-3. Monitor Register Bit Identification and Bit Functions (AN/TSQ-73) (Cont)

Bit Positions	Notes	S[1]	C[2]	L[3]	Function
14		X		X	IOC time out - 256 microseconds (IOC failed to honor real-time clock request)
15		X		X	Program time out - 1024 microseconds (set by IOC, real-time clock zero not initialized, or Mode 0 in keyword)
16	4, 5, 6				Not used (I/O avalanche error; multiple I/O errors)
17-20	4, 5, 6				Not used (MCMU bank address; for I/O data transfers only, keywords and termination words remain in base memory bank)
21-24					Memory bank address when IOC detects a memory parity error, access violation occurs, or time out (bit 21 is ZERO, bit 22 is MSB of memory address)
25-31					Device address (when any peripheral device error occurs, bit 25 is MSB of peripheral device address)

[1] S = Status portion of ADP Status and Control Panel

[2] C = Control portion of ADP Status and Control Panel

[3] L = Stimulates program level 2

[4] Used in TACFIRE

[5] Used in AN/TTC-39

[6] Used in NICS-TARE

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Table 4-IVB-4. Monitor Register Error Conditions for Bit Positions 1 and 2 (AN/TSQ-73)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set	
			Monitor Register	Query Register
1 and 2	Device response time out - 10 microseconds (device hung up; set by IOC)	Yes	9	
1 and 2	I/O memory parity error on control word (set by IOC)	Yes	11	
1 and 2	I/O memory parity error on data word (set by IOC)	Yes	12	
1 and 2	Memory time out - 60 microseconds (set by IOC)	Yes	13	
1 and 2	IOC time out - 256 microseconds (IOC failed to honor real-time clock request)	Yes	14	
1 and 2	Program time out - 1024 microseconds (set by IOC, real-time clock zero not initialized, or Mode 0 in keyword)	Yes	15	
2 only	Input on output error (set by IOC)	Yes	7	
2 only	I/O memory access violation (set by IOC)	Yes	10	
2 only	Instruction parity error (set by primary CPU)	Yes	0	
2 only	Level change parity error (set by primary CPU)	Yes	1	

Note 1: Bit Position 1, IOU Fault (System Fault)
Bit Position 2, Primary CPU Fault (Computer Fault)
Bit Position 6, Secondary CPU Fault

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Table 4-IVB-4. Monitor Register Error Conditions for Bit Positions 1 and 2 (AN/TSQ-73) (Cont)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level[2]	Other Bit Positions Being Set	
			Monitor Register	Query Register
2 only	Instruction violation set by primary CPU)	Yes		2
2 only	Memory access violation (set by primary CPU)	Yes		3
2 only	Memory time out (set by primary CPU)	Yes		4
2 only	Specification violation (set by primary CPU)	Yes		5
2 only	Instruction parity error (set by secondary CPU)	Yes		0
2 only	Level change parity error (set by secondary CPU)	Yes		1
2 only	Instruction violation (set by secondary CPU)	Yes		2
2 only	Memory access violation (set by secondary CPU)	Yes		3
2 only	Memory time out (set by secondary CPU)	Yes		4
2 only	Specification violation (set by secondary CPU)	Yes		5

Note 1: Bit Position 1, IOU Fault (System Fault)
Bit Position 2, Primary CPU Fault (Computer Fault)
Bit Position 6, Secondary CPU Fault

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Table 4-IVB-5. Maintenance Register (AN/TSQ-73)(Read with ITR Instruction, Device Address 02)

Bit Position	Indicator	Remarks
0-2	Not Used	
3	None	Environmental ZERO = one of the environmental fault condition exists.
4	None	Voice Communication Central Panel. ONE = indicates fault condition.
5	None	Main Power ZERO = One of the main power fault condition exists.
6	Primary CPU Select	ZERO = lower CPU is primary CPU ONE = upper CPU is primary CPU
7-9	Not Used	
10	IOX - 1	
11	IOX - 2	
12	IOX - 3	Indicate ON-LINE condition
13	IOM	
14	KPU	
15	Not Used[1]	(Continuity)[1]
16-21	PROGRAM TEST[2, 3, 4] (TEST thumbwheel)	Bit positions 16 to 18 associated most significant thumbwheel, bit positions 19 to 21 associated with least significant thumbwheel (64 selections).
22-24	Not Used[1]	(Define memory bank to be base memory)[1]
25-31	Not Used[1, 3, 4]	(ACC thumbwheel)[1] (Processor 1/2)[4] (PROGRAM LOAD rotary device select)[3,4]

[1] Used in TACFIRE

[2] Used in AN/TSQ-73

[3] Used in AN/TTC-39

[4] Used in NICS-TARE

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4-13C. ADP Status and Control Panel (AN/TTC-39)

The AN/TTC-39 has one front panel, called the Automatic Data Processor (ADP) Status and Control Panel. It consist of:

a. Status portion

b. Control portion

The ADP Status and Control panel of the computer contains the controls and indicators required by an operator to initialize and monitor system operation. The controls and indicators are arranged in functional groups for rapid identification of individual switch functions.

The Status portion of the ADP Status and Control Panel is shown in figure 4-IIIC-2. Table 4-IVC-1 identifies and specifies the functions of the control switches and corresponding indicator lights located on the Status portion of the ADP Status and Control Panel.

The Control portion of the ADP Status and Control Panel is shown in figure 4-IVC-1. Table 4-IVC-2 identifies, describes, and specifies the functions of the control switches and corresponding lights located on the Control portion of the ADP Status and Control Panel.

The AN/TTC-39 consists of Message Switches and Circuit Switches. The ADP Status and Control Panel for the two types of switches are similar. Figures 4-IIIC-2 and 4-IVC-1 and tables 4-IVC-1 and 4-IVC-2 are applicable for the Message Switch.

For the Circuit Switch, the program load, rotary device select is eliminated. The interface control has only one IFCU, ON/FAULT indicator pair. All other status and controls are identical to the Message Switch. (IFCU = Interface Control Unit.)

A discussion of the functional operation of the ADP Status and Control Panel for the message switch is presented in the subsequent paragraphs.

4-14C. Indicators and Controls (AN/TTC-39)

a. *Setting and Resetting of the ADP Status and Control Panel Control Indicators.* Many of the status and control indicators to be discussed will be programmable. All such indicators have a bit in the monitor register associated with them. In all cases, when the bit in the monitor register is ZERO, the monitor register indicator light is extinguished. However, if the bit in the monitor register is a ONE, the monitor register light remains illuminated. All bits of the monitor register are programmable. The bits of the monitor register (table 4-IVC-3) are set and reset as specified in table 4-IVA-5.

b. *Program Interrogation of the ADP Status and Control Panel.* All controls and corresponding indicator lights on the ADP Status and Control Panel have either a flip-flop circuit in the monitor register associated with them or they have an inherent storage capability of their own. In either case, all controls and corresponding indicator lights can be interrogated by the computer program using the ITR instruction (refer to table 4-IVA-5).

c. *ADP Status and Control Panel Initiated Interrupts.* The program test pushbutton, START, on the ADP Status and Control Panel interrupts the computer (monitor register bit position 5). The interrupt is associated with device address 02. The keyword and termination word associated with device address 02 are located as specified in table 4-IVA-6.

4-15C. Monitor Register (AN/TTC-39)

The monitor register of the input output controller (IOC) contains information pertaining to error conditions detected by the IOC. It also contains information pertaining to bootstrap program load and indicates when the instruction controller has posted a bit in the query register. Table 4-IVC-3 identifies and specifies the functions of each bit in the monitor register.

Input to register (ITR) instruction with peripheral device address 01 can read the monitor register. Output from register (OFR) instruction with peripheral device address 02 selectively resets bits in the monitor register. Output from register (OFR) instruction with peripheral device address 01 selectively sets bits in the monitor register, see table 4-IVA-5.

The setting of specific bits in the monitor register (table 4-8C) causes a program interrupt. The interrupt uses peripheral device address 02 termination word to stimulate a program level. The memory locations for the keyword and termination word for peripheral device address 02 are shown in table 4-IVA-6.

Table 4-IVC-3 also lists the monitor register bit positions which are displayed on the front panel and being affected by front panel pushbuttons; see also description of ADP Status and Control Panel (figures 4-IIIC-2 and 4-IVC-1 and tables 4-IVC-1 and 4-IVC-2).

Subsequent paragraphs describe the functions of the bit positions in the monitor register:

a. *Not Used, Bit Position 0.* This bit position is used only in TACFIRE. Pressing a pushbutton causes a computer interrupt using peripheral device address 02.

b. *System Fault, Bit Position 1.* This bit is set as a result of the setting of bits in the monitor register, as shown in table 4-IVC-4.

Table 4-IVC-1. Switch/Indicator Functions on Status Portion of ADP Status and Control Panel (AN/TTC-39)

Switch/Indicator	Description	Function
PROGRAM LOAD Rotary device select	Six position rotary switch (present in Message Switch, absent in Circuit Switch)	Selects the peripheral device to perform a program load when the PROG LOAD pushbutton is pressed. Peripheral device address depends upon least significant PROGRAM TEST thumbwheel switch (E = even, 0 = odd) and PROGRAM LOAD rotary switch E/TAPE A = 10* or O/TAPE A = 30* E/TAPE B = 11 O/TAPE B = 31 E/TAPE C = 12 O/TAPE C = 32 E/TAPE D = 13 O/TAPE D = 33 E/DISC A = 14 O/DISC A = 34 E/DISC B = 15 O/DISC B = 35 10 to 15 on IOE, operational 30 to 35 on IOX, system test
PROG LOAD	Momentary action pushbutton with white indicator (Program Load)	Pressing the pushbutton initiates a program load operation (monitor register bit position 4).
STATUS IOU/CPU	Amber indicators (2)	Indicate a fault in the IOU or CPU during program load.
DIAGNOSE CODE	Six octal digits light emitting diodes	Indicate diagnose code or fault number detected during program load or by software (diagnose register bit positions 16 through 31, 9, and 10, diagnose option 2).
STATUS IOU/CPU	Amber indicators (2)	Indicate fault detected in IOU or CPU (diagnose option 3).
RESTART	Momentary action pushbutton switch, nonilluminated white switch cap	Activation causes an interrupt to program level 1; similar to restart after power failure.
STOPPED	Red indicator	Indicates when CPU is stopped.

*Only for Circuit Switch

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Table 4-IVC-1. Switch/Indicator Functions on Status Portion of ADP Status and Control Panel (AN/TTC-39) (Cont)

Switch/Indicator	Description	Function
FAULT MEMORY PARITY/ T-OUT	Amber indicators (2) (Time Out)	Indicate a detected memory parity error by the CPU (query register bit positions 0 or 1) or by the IOU (monitor register bit positions 11 or 12) and a detected memory time out by the CPU (query register bit position 4) or by the IOU (monitor register bit position 13).
TIME OUT IOU/ PROG	Amber indicators (2) (Program)	Indicate the IOU failed to honor a real-time clock request in 256 microseconds (monitor register bit position 14) and program failed to initialize keyword for real-time clock 0 in 1024 microseconds or when Mode 0 in keyword is encountered (monitor register bit position 15).
DEVICE ERROR PARITY/ T-OUT	Amber indicators (2) (Time Out)	Indicate peripheral device input parity error, set by IOC (monitor register bit position 8) and peripheral device failed to respond to the IOC within 10 microseconds (monitor register bit position 9).
DEVICE ADDRESS	Two octal digits, light emitting diodes	Indicate peripheral device address when an I/O error has been detected (monitor register bit positions 26 to 31).
DEVICE ADDRESSES	Decal	List the peripheral device address assignments.

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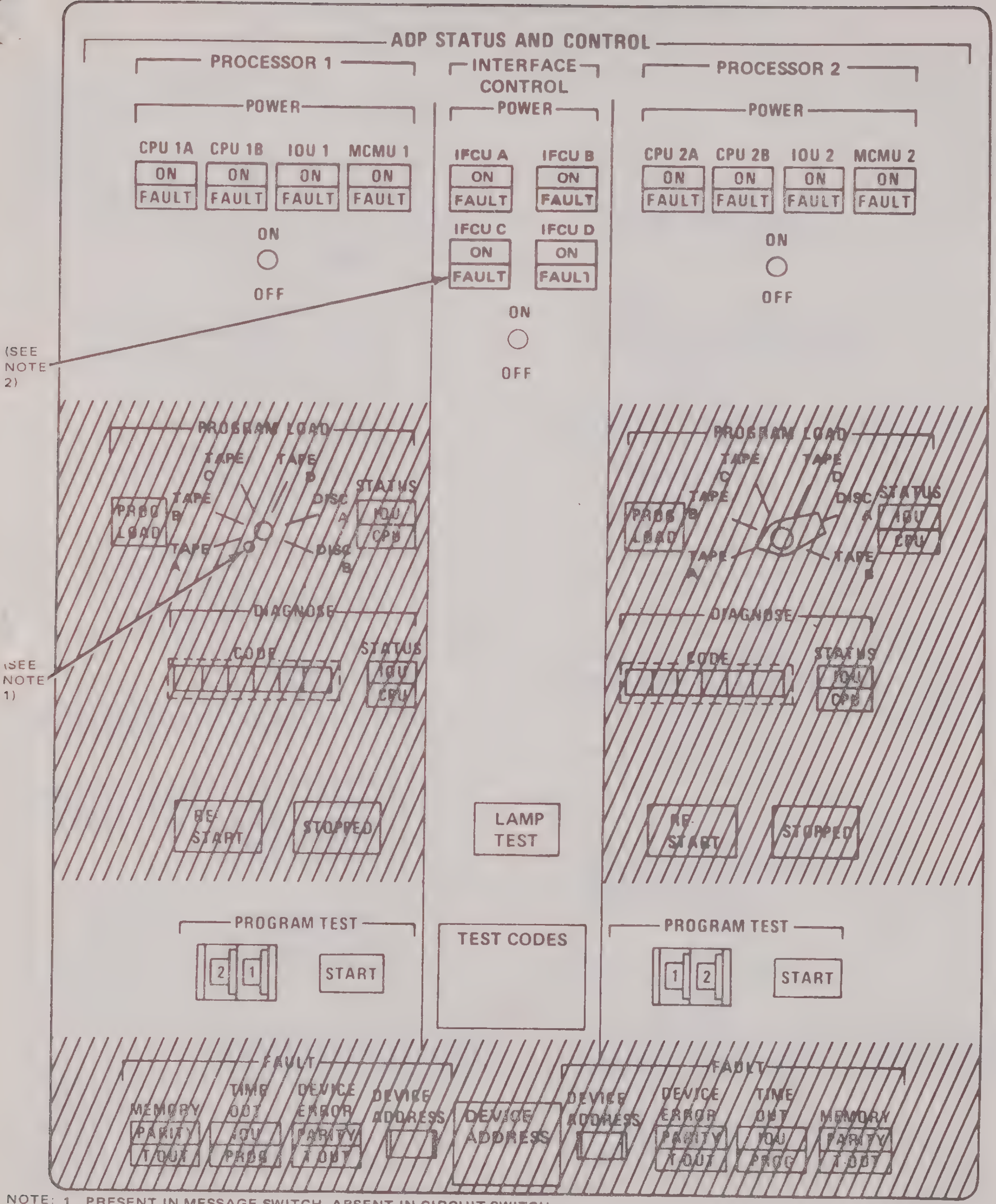
ADP STATUS AND CONTROL
PROCESSOR 1
INTERFACE CONTROL
PROCESSOR 2
POWER
CPU 1A
CPU 1B
IOU 1
MCMU 1
ON
FAULT
ON
OFF
IFCU A
IFCU B
IFCU C
IFCU D
CPU 2A
CPU 2B
IOU 2
MCMU 2
(SEE NOTE 2)
PROGRAM LOAD
TAPE C
TAPE D
TAPE B
TAPE A
DISC A
DISC B
PROG LOAD
STATUS
IOU
CPU
(SEE NOTE 1)
DIAGNOSE
CODE
RE-START
STOPPED
LAMP TEST
PROGRAM TEST
2
1
START
TEST CODES
FAULT
MEMORY
PARITY
T OUT
TIME OUT
IOU
PROG
DEVICE ERROR
DEVICE ADDRESS

NOTE: 1. PRESENT IN MESSAGE SWITCH, ABSENT IN CIRCUIT SWITCH.
2 FOUR IFCU IN MESSAGE SWITCH, ONE IFCU IN CIRCUIT SWITCH.

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Figure 4-IVC-1. Control Portion of ADP Status and Control Panel (AN/TTC-39)

Table 4-IVC-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (AN/TTC-39)

Switch/Indicator	Description	Function
PROCESSOR 1 POWER CPU 1A ON/FAULT	Green/red indicators (2) (CPU 1A)	Indicate power on CPU 1A / power fault in CPU 1A power supply.
CPU 1B ON/FAULT	Green/red indicators (2)	Indicate power on CPU 1B / power fault in CPU 1B power supply.
IOU 1 ON/FAULT	Green/red indicators (2) (IOU 1)	Indicate power on IOU 1 / power fault in IOU 1 power supply.
MCMU 1 ON/FAULT	Green/red indicators (2) (Mass Core Memory Unit 1)	Indicate power on MCMU 1 / power fault in MCMU 1 power supply.
ON/OFF	Two-position toggle switch	Power switch to CPU 1A, CPU 1B, IOU 1, MCMU 1.
PROGRAM TEST XX	Two-octal thumbwheel switches (00 to 77)	Indicate program test number (maintenance register bit positions 16 to 21) or program load peripheral device address: XE = address 10 to 15, IOE (operational) XO = address 30 to 35, IOX (system test) X = don't care E = even, 0 = odd Also, see PROGRAM LOAD switch.
START	Momentary action pushbutton	Pressing of the pushbutton sets bit position 5 in the monitor register, illuminates indicator, and interrupts the computer using peripheral device address 02. Program resets this bit position.

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Table 4-IVC-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (AN/TTC-39) (Cont)

Switch/Indicator	Description	Function
INTERFACE CONTROL POWER IFCU A ON/FAULT	Green/red indicators (2) (ICU A)	Indicate power on IFCU A / power fault in IFCU A power supply.
IFCU B ON/FAULT	Green/red indicators (2) (present in Message Switch; absent in Circuit Switch)	Indicate power on IFCU B / power fault in IFCU B power supply.
IFCU C ON/FAULT	Green/red indicators (2) (present in Message Switch; absent in Circuit Switch)	Indicate power on IFCU C / power fault in IFCU C power supply.
IFCU D ON/FAULT	Green/red indicators (2) (present in Message Switch; absent in Circuit Switch)	Indicate power on IFCUD / power fault in IFCU D power supply.
ON/OFF	Two-position toggle switch	Power switch to all IFCU.
LAMP TEST	Momentary action pushbutton switch	Applies power to all indicators on ADP Status and Control Panel.
TEST CODES	Decal	
PROCESSOR 2	Same as processor 1	Same as processor 1

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Table 4-IVC-3. Monitor Register Bit Identification and Bit Functions (AN/TTC-39)

Bit Positions	Notes	S[1]	C[2]	L[3]	Function
00	4, 5				Not used (computer interrupt)
01	6			X	System fault
02	6			X	Computer fault
03	4, 7				Not used (program load channel 11)
04		X			Program load
05	5		X		Start (program test)
06	7				Not used (secondary CPU fault)
07					Input on output error (set by IOC)
08		X			Device input parity error (set by IOC)
09		X		X	Device time out - 10 microseconds (peripheral device hung up, set by IOC)
10				X	I/O memory access violation (set by IOC)
11	8	X		X	I/O memory parity error on control word (set by IOC)
12	8	X		X	I/O memory parity error on data word (set by IOC)
13		X		X	Memory time out - 60 microseconds (set by IOC)

[1] S = Status portion of ADP Status and Control Panel

[2] C = Control portion of ADP Status and Control Panel

[3] L = Stimulates program level 2

[4] Used in TACFIRE

[5] Pressing these buttons causes an interrupt

[6] See table 4-IVC-4 for all conditions which set these bits

[7] Used in AN/TSQ-73

[8] ORed, one indicator, also, ORed with query register bit positions 0 and 1

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Table 4-IVC-3. Monitor Register Bit Identification and Bit Functions (AN/TTC-39) (Cont)

Bit Positions	Notes	S[1]	C[2]	L[3]	Function
14		X		X	IOC time out - 256 microseconds (IOC failed to honor real-time clock request)
15		X		X	Program time out - 1024 microseconds (set by IOC, real-time clock zero not initialized, or Mode 0 in keyword)
16					I/O avalanche error (multiple I/O errors)
17-20					MCMU bank address (for I/O data transfers only, key words and termination words remain in base memory bank)
21-24					Memory bank address when memory IOC detects a parity error, access violation occurs, or time out (bit 21 is ZERO, bit 22 is MSB of memory address)
25-31		X			Device address (when any peripheral device error occurs, bit 25 is ZERO, bit 26 is MSB of peripheral device address)

[1] S = Status portion of ADP Status and Control Panel

[2] C = Control portion of ADP Status and Control Panel

[3] L = Stimulates program level 2

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c. *Computer Fault, Bit Position 2.* This bit position is set as a result of the setting of bits in the monitor register, query register, and indicator register as shown in table 4-IVC-4.

d. *Not Used, Bit Position 3.* This bit position is used only in TACFIRE and AN/TSQ-73. Pressing a pushbutton causes a program load for channel 11.

e. *Program Load, Bit Position 4.* This bit is set when the PROGRAM LOAD button, PROG LOAD, is pressed.

f. *Start, Bit Position 5.* This bit is set when the PROGRAM TEST button, START, is pressed. It causes a computer interrupt using peripheral device address 02. The test to be performed can be specified by the two program test thumbwheels. The thumbwheels are connected to the maintenance register which can be read by an ITR instruction with peripheral device address 02.

g. *Not Used, Bit Position 6.* This bit position is ed only in AN/TSQ-73. It indicates a secondary CPU lt.

h. *Input on Output Error, Bit Position 7.* This bit is set when a peripheral device inputs data while the keyword specifies output, modes 1, 4, and 5.

i. *Device Input Parity Error, Bit Position 8.* This bit is set when an input parity error occurs during bootstrap program load (IOC will be stopped).

This bit is also set when an input parity error is detected during automatic input and the P-bit in the termination word is a ONE. The program level (EPL) as specified in the termination word will be stimulated (not program level 2, unless EPL = 2).

j. *Device Time Out, Bit Position 9.* This bit is set when a peripheral device time out occurs during an I/O operation (peripheral device hang up). This bit is set when a peripheral device is not responding to the IOC's address/enable sequence within 10 microseconds in the automatic input mode. An automatic transfer to program level 2 is also initiated.

Table 4-IVC-4. Monitor Register Error Conditions for Bit Positions 1 and 2 (AN/TTC-39)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set		
			Monitor Register	Query Register	Indicator Register
1 and 2	Device response time out - 10 microseconds (device hung up, set by IOC)	Yes	9		
1 and 2	I/O memory parity error on control word (set by IOC)	Yes	11		
1 and 2	I/O memory parity error on data word (set by IOC)	Yes	12		
1 and 2	Memory time out - 60 microseconds (set by IOC)	Yes	13		
1 and 2	IOC time out - 256 microseconds (IOC failed to honor real time clock request)	Yes	14		
1 and 2	Program time out - 1024 microseconds (set by IOC, real time clock zero not initialized, or Mode 0 in keyword)	Yes	15		
2 only	Input on output error (set by IOC)	Yes	7		
2 only	I/O memory access violation (set by IOC)	Yes	10		
2 only	Instruction parity error (set by CPU)	Yes		0	
2 only	Level change parity error by CPU)	Yes		1	

NOTE 1: Bit Position 1, System Fault
Bit Position 2, Computer Fault

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Table 4-IVC-4. Monitor Register Error Conditions for Bit Positions 1 and 2 (AN/TTC-39) (Cont)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set		
			Monitor Register	Query Register	Indicator Register
2 only	Instruction violation (set by CPU)	Yes		2	
2 only	Memory access violation (set by CPU)	Yes		3	
2 only	Memory time out (set by CPU)	Yes		4	
2 only	Specification violation (set by CPU)	Yes		5	

NOTE 1: Bit Position 1, System Fault
Bit Position 2, Computer Fault

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k. *I/O Memory Access Violation, Bit Position 10.* This bit is set when a memory access violation occurs during an input or output operation.

An automatic transfer to program level 2 is also initiated. There is no indicator on the front panel.

l. *I/O Memory Parity Error on Control Word, Bit Position 11.* This bit is set when the IOC detects a memory parity error when accessing the base memory bank (keyword, termination word, program activity register, queue register).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 12 for display on the front panel.

m. *I/O Memory Parity Error on Data Word, Bit Position 12.* This bit is set when the IOC detects a memory parity error when accessing memory for data transfers (full word output, byte output, byte input).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 11 for display on the front panel.

n. *Memory Time Out, Bit Position 13.* This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request by the IOC.

An automatic transfer to program level 2 is also initiated.

o. *IOC Time Out, Bit Position 14.* This bit is set when the IOC fails to honor a real-time clock request (any of the three) within 256 microseconds.

An automatic transfer to program level 2 is also initiated.

p. *Program Time Out, Bit Position 15.* This bit is set when the IOC detects that the keyword block length field for the real-time clock zero (peripheral device address 03) is zero. The program should have reinitialized this field within 1,024 microseconds after it has been decremented to zero.

An automatic transfer to program level 2 is also initiated.

q. *I/O Avalanche Error, Bit Position 16.* The setting of any bit positions 7, 9 through 15 indicates that an error has occurred that stimulated program level 2. The setting of any one of these bit positions will set a flip-flop (not related to bit position 16) inhibiting any further setting until an OF instruction to peripheral device address 01 or 02 has been executed. This OFR instruction will enable the setting of bit positions 7, 9 through

15 in the monitor register; the OFR instruction is effective even when all bits in the selected process register are all zeros. The avalanche error, bit position 16 will be set when the IOC detects a second I/O related error before a first error (which stimulated program level 2) has been cleared by executing an OFR instruction to peripheral address 01 or 02.

r. *MCMU Bank Address, Bit Positions 17 through 20.* This 4-bit field specifies the Mass Core Memory Unit (MCMU) bank address to be used for I/O data transfers.

NOTE

The keywords and termination words remain in the base memory bank.

s. *Memory Bank Address, Bit Positions 21 through 24.* Bit position 21 is ZERO, bit position 22 is the most significant bit of the memory address. These bits are set when the IOC detects one of the following conditions:

(1) Memory parity error.

(2) Memory access violation.

(3) Memory time out.

(4) No update on second error.

t. *Device Address, Bit Positions 25 through 31.* Bit position 25 is ZERO, bit position 26 is the most significant bit of the peripheral device address. These bits are set when the IOC detects an error which cause to set any bit positions 9 through 15.

NOTE

The device address bits are also set under two conditions that do not stimulate program level 2. First, when an input parity error is detected during bootstrap program load, monitor register bit 8 will be set and the IOC stops. Second, when an input parity error is detected during an automatic input and the P-bit in the termination word is a ONE. The program level (EPL), as specified in the termination word, will be stimulated (not program level 2, unless EPL = 2); the device address may be ambiguous for this second case.

4-16C. Maintenance Register (AN/TTC-39)

The maintenance register is an extension of the monitor register. This register uses only control inputs from switches or control lines. Thus, the register can be read by the computer but bits cannot be reset. Bits are changed by changing thumbwheel switches and control lines.

Table 4-IVC-5 lists the bit positions and functions assigned to the maintenance register. The maintenance register can be read by the computer using an ITR instruction with peripheral device address 02.

4-17C. Special Input/Output (I/O) Addresses (AN/TTC-39)

Table 4-IVA-8 lists the functions of the special I/O addresses listed in table 4-2.

Table 4-IVC-5. Maintenance Register (AN/TTC-39) (Read with ITR Instruction, Device Address 02)

Bit Positions	Indicator	Remarks
0-14	Not used[1]	
15	Not used[2]	
16-21	PROGRAM TEST[1,3,4] (TEST thumbwheel)[2]	Indicate program test number. Bit positions 16 to 18 associated with most significant thumbwheel; bit positions 19 to 21 associated with least significant thumbwheel (64 selections or program load peripheral device address: XE = address 10 to 15, IOE (operational) XO = address 30 to 35, IOX (system test) X = Don't care E = even, O = odd Also, see PROGRAM LOAD switch.
22-24	Not used[2]	(Define memory bank to be base memory)[2]
25-28	Not used[2]	(See Below)[2]
27	Not used[4]	(Processor 1/2)[4]
29-31	PROGRAM LOAD rotary device select[3]	Circuit Switch[3]: Not used Message Switch only[3] Least significant octal digit of peripheral device address: TAPE A = 0 TAPE B = 1 TAPE C = 2 TAPE D = 3

[1] Used in AN/TSQ-73

[2] Used in TACFIRE

[3] Used in AN/TTC-39

[4] Used in NICS-TARE

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Table 4-IVC-5. Maintenance Register (AN/TTC-39) (Read with ITR Instruction, Device Address 02) (Cont)

Bit Positions	Indicator	Remarks
29-31 (Cont)	PROGRAM LOAD rotary device select[3] (Cont)	DISC A = 4 DISC B = 5 More significant ocatal digit determined by least significant PROGRAM TEST thumbwheel: XE = address 10 to 15, IOE (operational) XO = address 30 to 35, IOX (system test) X = Don't care E = Even, O = Odd
25-31	(ACC ADDRESS)[2]	

[1] Used in AN/TSQ-73

[2] Used in TACFIRE

[3] Used in AN/TTC-39

[4] Used in NICS-TARE

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4-13D. ADP Status and Control Panel (NICS-TARE)

NICS-TARE has 2 front panels, one for each computer, called the Automatic Data Processor (ADP) Status and Control Panel. It consists of:

a. Status portion

b. Control portion

The ADP Status and Control Panel of the computer contains the controls and indicators required by an operator to initialize and monitor system operation. The controls and indicators are arranged in functional groups for rapid identification of individual switch functions.

The Status portion of the ADP Status and Control Panel is shown in figure 4-IIID-2. Table 4-IVD-1 identifies and specifies the functions of the control switches and corresponding indicator lights located on the Status portion of the ADP Status and Control panel.

The Control portion of the ADP Status and Control Panel is shown in figure 4-IVD-1. Table 4-IVD-2 identifies, describes, and specifies the functions of the control switches and corresponding lights located on the Control portion of the ADP Status and Control Panel.

A discussion of the functional operation of the ADP Status and Control Panel is presented in the subsequent paragraphs.

4-14D. Indicators and Controls (NICS-TARE)

a. *Setting and Resetting of the ADP Status and Control Panel Control Indicators.* Many of the status and control indicators to be discussed will be programmable. All such indicators have a bit in monitor register associated with them. In all cases, when the bit in the monitor register is ZERO, the monitor register indicator light is extinguished. However, if the bit in the monitor register is a ONE, the monitor register light remains illuminated. All bits of the monitor register are programmable. The bits of the monitor register (table 4-IVD-3) are set and reset as specified in table 4-10A.

b. *Program Interrogation of the ADP Status and Control Panel.* All controls and corresponding indicator lights on the ADP Status and Control Panel have either a flip-flop circuit in the monitor register associated with them or they have an inherent storage capability of their own. In either case, all controls and corresponding indicator lights can be interrogated by the computer program using the ITR instruction (refer to table 4-IVA-5).

c. *ADP Status and Control Panel Initiated Interrupts.* The PROGRAM TEST pushbutton, START, on the ADP Status and Control Panel interrupts the computer (monitor register bit position 5). The interrupt is associated with device address 02. The keyword and termination word associated with device address 02 are located as specified in table 4-IVA-6.

4-15D. Monitor Register (NICS-TARE)

The monitor register of the input output controller (IOC) contains information pertaining to error conditions detected by the IOC. It also contains information pertaining to bootstrap program load and indicates when the instruction controller has posted a bit in the query register. Table 4-IVD-3 identifies and specifies the functions of each bit in the monitor register.

Input to register (ITR) instruction with peripheral device address 01 can read the monitor register. Output from register (OFR) instruction with peripheral device address 02 selectively resets bits in the monitor register. Output from register (OFR) instruction with peripheral device address 01 selectively sets bits in the monitor register, see table 4-IVA-5.

The setting of specific bits in the monitor register (table 4-IVD-3) causes a program interrupt. The interrupt uses peripheral device address 02 termination word to stimulate a program level. The memory locations for the keyword and termination word for peripheral device address 02 are shown in table 4-IVA-6.

Table 4-IVD-3 also lists the monitor register bit positions which are displayed on the front panel and being affected by front panel pushbuttons; see also description of ADP Status and Control Panel (figures 4-IIID-2 and 4-IVD-1 and tables 4-IVD-1 and 4-IVD-2).

Subsequent paragraphs describe the functions of the bit positions in the monitor register:

a. *Not Used, Bit Position 0.* This bit position is used only in TACFIRE. Pressing a pushbutton causes a computer interrupt using peripheral device address 02.

b. *System Fault, Bit Position 1.* This bit is set as a result of the setting of bits in the monitor register, as shown in table 4-IVD-4.

c. *Computer Fault, Bit Position 2.* This bit position is set as a result of the setting of bits in the monitor register, and query register as shown in table 4-IVD-4.

d. *Not Used, Bit Position 3.* This bit position is used only in TACFIRE and AN/TSQ-73. Pressing of a pushbutton causes a program load for channel 11.

e. *Program Load, Bit Position 4.* This bit is set when the PROGRAM LOAD button, PROG LOAD, is pressed.

f. *Start, Bit Position 5.* This bit is set when the PROGRAM TEST button, START, is depressed. It causes a computer interrupt using peripheral device address 02. The test to be performed can be specified by

Table 4-IVD-1. Switch/Indicator Functions on Status Portions of ADP Status and Control Panel (NICS-TARE)

Switch/Indicator	Description	Function
PROGRAM LOAD Rotary device select	Two-position rotary switch	Selects the peripheral device to perform a program load when the PROG LOAD pushbutton is pressed. Peripheral device address depends upon most significant PROGRAM TEST thumbwheel switch (1, 4, 5, 6, or 7) and PROGRAM LOAD rotary switch 1/DISC A = 10 1/DISC B = 11 4/DISC A = 40 4/DISC B = 41 5/DISC A = 50 5/DISC B = 51 6/DISC A = 60 6/DISC B = 61 7/DISC A = 70 7/DISC B = 71 10 and 11 on IOE, operational 40 to 61 on IOE, system test 70 and 71 on IOX, system test
PROG LOAD	Momentary action pushbutton with white indicator (Program Load)	Pressing of the pushbutton initiates a program load operation (monitor register bit position 4).
STATUS IOU/CPU	Amber indicators (2)	Indicate a fault in the IOU or CPU during program load.
DIAGNOSE CODE	Six octal digits light emitting diodes	Indicate diagnose code or fault number detected during program load or by software (diagnose register bit positions 16 through 31, 9, and 10, diagnose option 2).
STATUS IOU/CPU	Amber indicators (2)	Indicate fault detected in IOU or CPU diagnose option 3).
RESTART	Momentary action pushbutton switch, nonilluminated white switch cap	Activation causes an interrupt to program level 1; similar to restart after power failure.
STOPPED	Red indicator	Indicates when CPU is stopped.

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Table 4-IVD-1. Switch/Indicator Functions on Status Portions of ADP Status and Control Panel (NICS-TARE) (Cont)

Switch/Indicator	Description	Function
FAULT DEVICE ADDRESS	Two octal digits, light emitting diodes	Indicate peripheral device address when an I/O error has been detected (monitor register bit positions 26 to 31)
DEVICE ERROR PARITY/ T-OUT	Amber indicators (2)	Indicate peripheral device input parity error, set by IOC (monitor register bit position 8) and peripheral device failed to respond to the IOC within 10 microseconds (monitor register bit position 9)
TIME OUT IOU/ PROG	Amber indicators (2) (Program)	Indicate the IOU failed to honor a real-time clock request in 2048 microseconds (monitor register bit position 14) and program failed to initialize keyword for real-time clock 0 in 8192 microseconds or when Mode 0 in keyword is encountered (monitor register bit position 15)
MEMORY PARITY T-OUT	Amber indicators (2) (Time Out)	Indicate a detected memory parity error by the CPU (query register bit positions 0 or 1) or by the IOU (monitor register bit positions 11 or 12) and a detected memory time out by the CPU (query register bit position 4) or by the IOU (monitor register bit position 13).

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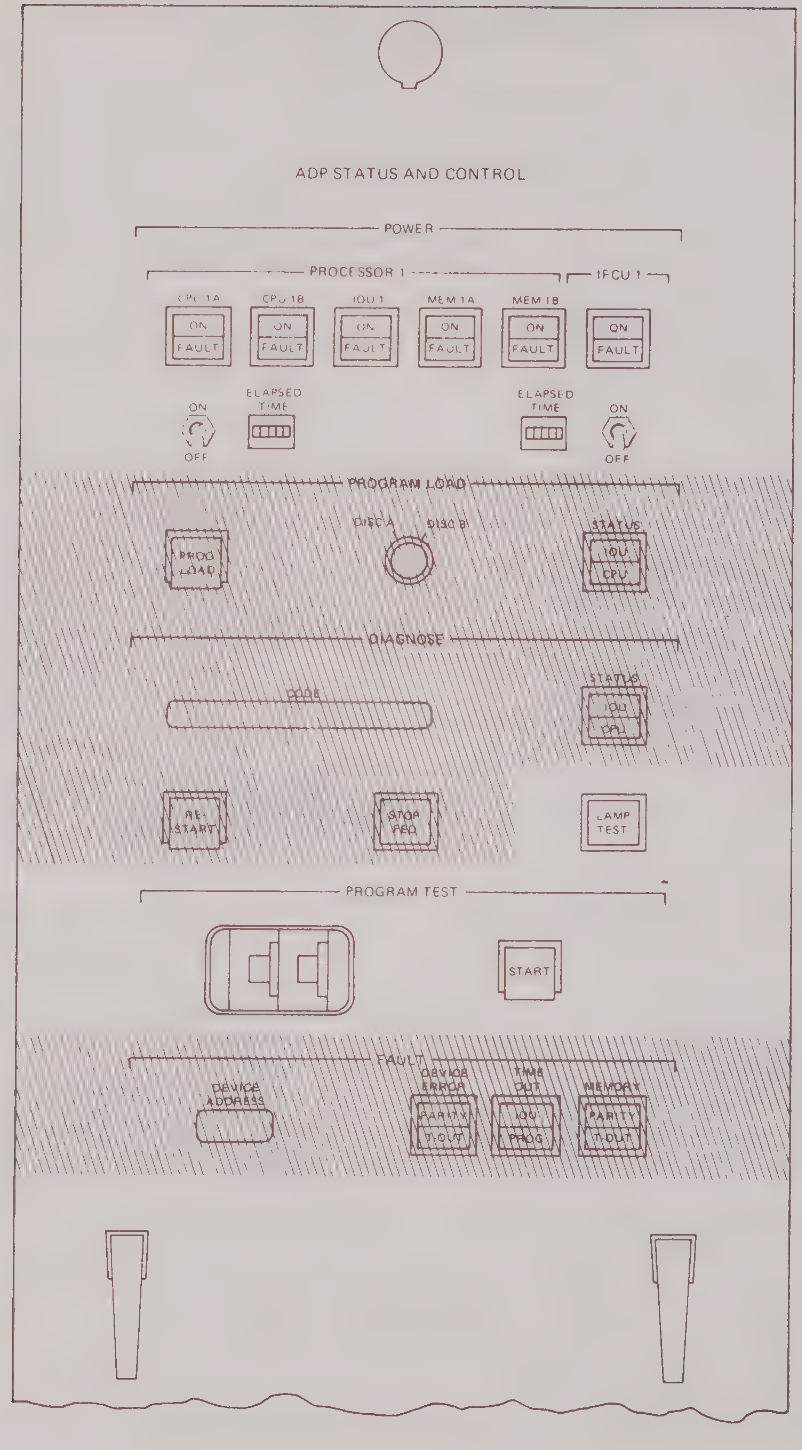
ADP STATUS AND CONTROL
POWER
PROCESSOR 1
IFCU 1
CPU 1A
CPU 1B
IOU 1
MEM 1A
MEM 1B
ON
FAULT
ELAPSED TIME
ON
OFF
PROGRAM LOAD
PROG LOAD
DISC A
DISC B
STATUS
IOU
CPU
DIAGNOSE
CODE
RE-START
STOP PRO
LAMP TEST
PROGRAM TEST
START
FAULT
DEVICE ADDRESS
DEVICE ERROR
TIME OUT
MEMORY
PARITY
T-OUT
IOU
PROG

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Figure 4-IVD-1. Control Portion of ADP Status and Control Panel (NICS-TARE)

Table 4-IVD-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (NICS-TARE)

Switch/Indicator	Description	Function
POWER IFCU 1 ON/FAULT	Green/red indicators (2) (ICU 1)	Indicate power on IFCU 1/power fault in IFCU 1 power supply.
ELAPSED TIME	Meter	Measures elapsed time of IFCU 1.
ON/OFF	Two-position toggle switch	Power switch to IFCU 1.
LAMP TEST	Momentary action pushbutton switch	Applies power to all indicators on ADP Status and Control Panel.
PROGRAM TEST XX	Two octal thumbwheel switches (00 to 77)	Indicate program test number (maintenance register bit positions 16 to 21) or program load peripheral device address: 1X = address 10 or 11, IOE (operational) 4X = address 40 or 41, IOE 5X = address 50 or 51, IOE 6X = address 60 or 61, IOE 7X = address 70 or 71, IOX (system test) X = Don't care
START	Momentary action pushbutton with white indicator	Pressing of the pushbutton sets bit position 5 in the monitor register, illuminates indicator, and interrupts the computer using peripheral device address 02. Program resets this bit position.
PANEL 2	Same as Panel 1	Same as Panel 1

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Table 4-IVD-2. Switch/Indicator Functions on Control Portion of ADP Status and Control Panel (NICS-TARE) (Cont)

Switch/Indicator	Description	Function
POWER PROCESSOR I CPU 1A ON/FAULT	Green/red indicators (2) (Central Processing Unit 1A)	Indicate power on CPU 1A/power fault in CPU 1A power supply.
CPU 1B ON/FAULT	Green/red indicators (2)	Indicate power on CPU 1B/power fault in CPU 1B power supply.
IOU 1 ON/FAULT	Green/red indicators (2) (Input-Output Unit 1)	Indicate power on IOU 1/power fault in IOU 1 power supply.
MEM 1A ON/FAULT	Green/red indicators (2) (Mass Core Memory Unit 1A)	Indicate power on MEM 1A/power fault in MEM 1A power supply.
MEM 1B	Green/red indicators (2) (Mass Core Memory Unit 1B) (spare)	Indicate power on MEM 1B/power fault in MEM 1B power supply.
ON/OFF	Two-position toggle switch	Power switch to CPU 1A, CPU 1B, IOU 1, MCMU 1A, MCMU 1B.
ELAPSED TIME	Meter	Measures elapsed time of processor 1 (CPU 1A, CPU 1B, MEM 1A, MEM 1B).

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Table 4-IVD-3. Monitor Register Bit Identification and Bit Functions (NICS-TARE)

Bit Position	Notes	S[1]	C[2]	L[3]	Function
00	4, 5				Not used (computer interrupt)
01	6			X	System fault
02	6			X	Computer fault
03	4, 7				Not used (program load channel 11)
04		X			Program load
05	5		X		Start (program test)
06	7				Not used (secondary CPU fault)
07					Input on output error (set by IOC)
08		X			Device input parity error (set by IOC)
09		X		X	Device time out - 10 microseconds (peripheral device hung up, set by IOC)
10				X	I/O memory access violation (set by IOC)
11	8	X		X	I/O memory parity error on control word (set by IOC)
12	8	X		X	I/O memory parity error on data word (set by IOC)
13		X		X	Memory time out - 60 microseconds (set by IOC)

[1] S = Status portion of ADP Status and Control Panel

[2] C = Control portion of ADP Status and Control Panel

[3] L = Stimulates program level 2

[4] Used in TACFIRE

[5] Pressing of these buttons causes an interrupt

[6] See table 4-IVD-4 for all conditions which set these bits

[7] Used in AN/TSQ-73

[8] ORed, one indicator; also, ORed with query register bit positions 0 and 1

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Table 4-IVD-3. Monitor Register Bit Identification and Bit Functions (NICS-TARE) (Cont)

Bit Positions	Notes	S[1]	C[2]	L[3]	Function
14		X		X	IOC time out - 2048 microseconds (IOC failed to honor real-time clock request).
15		X		X	Program time out - 8192 microseconds (set by IOC, real time clock zero not initialized, or Mode 0 in keyword).
16					I/O avalanche error (multiple I/O errors).
17-20					MCMU bank address (for I/O data transfers only, key words and termination words remain in base memory bank).
21-24					Memory bank address when IOC detects a memory parity error, access violation occurs, or time out (bit 21 is ZERO, bit 22 is MSB of memory address).
25-31		X			Device address (when any peripheral device error occurs, bit 25 is ZERO, bit 26 is MSB of peripheral device address)

[1] S = Status portion of ADP Status and Control Panel

[2] C = Control portion of ADP Status and Control Panel

[3] L = Stimulates program level 2

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Table 4-IVD-4. Monitor Register Error Conditions for Bit Positions 1 and 2 (NICS-TARE)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set		
			Monitor Register	Query Register	Indicator Register
1 and 2	Device response time out - 10 microseconds device hung up, set by IOC)	Yes	9		
1 and 2	I/O memory parity error on control word (set by IOC)	Yes	11		
1 and 2	I/O memory parity error on data word (set by IOC)	Yes	12		
1 and 2	Memory time out - 60 microseconds (set by IOC)	Yes	13		
1 and 2	IOC time out - 2048 microseconds (IOC failed to honor real time clock request)	Yes	14		
1 and 2	Program time out - 8192 microseconds (set by IOC, real-time clock zero not initialized, or Mode 0 in keyword)	Yes	15		
2 only	Input on output error (set by IOC)	Yes	7		
2 only	I/O memory access violation (set by IOC)	Yes	10		
2 only	Instruction parity error (set by CPU)	Yes		0	
2 only	Level change parity error (set by CPU)	Yes		1	
2 only	Instruction violation (set by CPU)	Yes		2	

NOTE 1: Bit Position 1, System Fault
Bit Position 2, Computer Fault

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Table 4-IVD-4. Monitor Register Error Conditions for Bit Positions 1 and 2 (NICS-TARE) (Cont)

Monitor Register Bit Positions[1]	Error Condition Causing Bits to be Set	Enter Program Level 2	Other Bit Positions Being Set		
			Monitor Register	Query Register	Indicator Register
2 only	Memory access violation (set by CPU)	Yes		3	
2 only	Memory time out (set by CPU)	Yes		4	
2 only	Specification violation (set by CPU)	Yes		5	

NOTE 1: Bit Position 1, System Fault
Bit Position 2, Computer Fault

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the two program test thumbwheels. The thumbwheels are connected to the maintenance register which can be read by an ITR instruction with peripheral device address 02.

g. *Not Used, Bit Position 6.* This bit position is used only in AN/TSQ-73. It indicates a secondary CPU fault.

h. *Input on Output Error, Bit Position 7.* This bit is set when a peripheral device inputs data while the keyword specifies output, modes 1, 4, and 5.

i. *Device Input Parity Error, Bit Position 8.* This bit is set when an input parity error occurs during bootstrap program load (IOC will be stopped).

This bit is also set when an input parity error is detected during automatic input and the P-bit in the termination word is a ONE. The program level (EPL) as specified in the termination word will be stimulated (not program level 2, unless EPL = 2).

j. *Device Time Out, Bit Position 9.* This bit is set when a peripheral device time out occurs during an I/O operation (peripheral device hang up). This bit is set when a peripheral device is not responding to the IOC's address/enable sequence within 10 microseconds in the automatic input mode.

An automatic transfer to program level 2 is also initiated.

k. *I/O Memory Access Violation, Bit Position 10.* This bit is set when a memory access violation occurs during an input or output operation.

An automatic transfer to program level 2 is also initiated. There is no indicator on the front panel.

l. *I/O Memory Parity Error on Control Word, Bit Position 11.* This bit is set when the IOC detects a memory parity error when accessing the base memory bank (keyword, termination word, program activity register, queue register).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 12 for display on the front panel.

m. *I/O Memory Parity Error on Data Word, Bit Position 12.* This bit is set when the IOC detects a memory parity error when accessing memory for data transfers (full word output, byte output, byte input).

An automatic transfer to program level 2 is also initiated. This bit position is ORed with bit position 11 for display on the front panel.

n. *Memory Time Out, Bit Position 13.* This bit is set when a memory bank has failed to respond in 60 microseconds to a memory request by the IOC.

An automatic transfer to program level 2 is also initiated.

o. *IOC Time Out, Bit Position 14.* This bit is set when the IOC fails to honor a real-time clock request (any of the three) within 2,048 microseconds.

An automatic transfer to program level 2 is also initiated.

p. *Program Time Out, Bit Position 15.* This bit is set when the IOC detects that the keyword block length field for the real-time clock zero (peripheral device address 03) is zero. The program should have reinitialized this field within 8,192 microseconds after it has been decremented to zero.

An automatic transfer to program level 2 is also initiated.

q. *I/O Avalanche Error, Bit Position 16.* The setting of any bit positions 7, 9 through 15, indicates that an error has occurred that stimulated program level 2. The setting of any one of these bit positions will set a flip-flop (not related to bit position 16) inhibiting any further setting until an OFR instruction to peripheral device address 01 or 02 has been executed. This OFR instruction will enable the setting of bit positions 7, 9 through 15 in the monitor register; the OFR instruction is effective even when all bits in the selected process register are all zeros. The avalanche error, bit position 16 will be set when the IOC detects a second I/O related error before a first error (which stimulated program level 2) has been cleared by executing an OFR instruction to peripheral address 01 or 02.

r. *MCMU Bank Address, Bit Positions 17 through 20.* This 4 bit field specifies the Mass Core Memory Unit (MCMU) bank address to be used for I/O data transfers.

NOTE

The keywords and termination words remain in the base memory bank.

s. *Memory Bank Address, Bit Positions 21 through 24.* Bit position 21 is ZERO, bit position 22 is the most significant bit of the memory address. These bits are set when the IOC detects one of the following conditions:

(1) Memory parity error.

(2) Memory access violation.

(3) Memory time out.

(4) No update on second error.

t. *Device Address, Bit Positions 25 through 31.* Bit position 25 is ZERO, bit position 26 is the most significant bit of the peripheral device address. These bits are set when the IOC detects an error which cause to set any bit positions 9 through 15.

NOTE

The device address bits are also set under two conditions that do not stimulate program level 2. First, when an input parity error is detected during bootstrap program load, monitor register bit 8 will be set and the IOC stops. Second, when an input parity error is detected during an automatic input and the P-bit in the termination word is a ONE. The program level (EPL), as specified in the termination word, will be stimulated (not program level 2, unless EPL = 2); the device address may be ambiguous for this second case.

4-16D. Maintenance Register (NICS-TARE)

The maintenance register is an extension of the monitor register. This register uses only control inputs from switches or control lines. Thus, the register can be read by the computer but bits cannot be reset. Bits are changed by changing thumbwheel switches and control lines.

Table 4-IVD-5 lists the bit positions and functions assigned to the maintenance register. The maintenance register can be read by the computer using an ITR instruction with peripheral device address 02.

4-17D. Special Input/Output (I/O) Addresses (NICS-TARE)

Table 4-IVA-8 lists the functions of the special I/O addresses listed in table 4-2.

Table 4-IVD-5. Maintenance Register (NICS-TARE) (Read with ITR Instruction, Device Address 02)

Bit Positions	Indicator	Remarks
0-14	Not used[1]	
15	Not used[2]	
16-21	PROGRAM TEST[1,3,4] TEST thumbwheel[2]	Indicate program test number Bit positions 16 to 18 associated most significant thumbwheel, bit positions 19 to 21 associated with least significant thumbwheel (64 selections) or program load peripheral device address 1X = address 10 or 11, IOE (operational) 4X = address 40 or 41, IOE 5X = address 50 or 51, IOE 6X = address 60 or 61, IOE 7X = address 70 or 71, IOX (system test) X = Don't care
22-24	Not used[2]	(Define memory bank to be base memory)[2]
25, 26	Not used[2]	(See below)[2]
27	None[4]	Processor location ZERO = Processor 1 ONE = Processor 2
28	Not used[2]	(See below)[1]
29-31	PROGRAM LOAD rotary device select[3,4]	Least significant octal digit of peripheral device address: Disc A = 0 Disc B = 1

[1] Used in AN/TSQ-73

[2] Used in TACFIRE

[3] Used in AN/TTC-39

[4] Used in NICS/TARE

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Table 4-IVD-5. Maintenance Register (NICS-TARE) (Read with ITR Instruction, Device Address 02) (Cont)

Bit Positions	Indicator	Remarks
29-31 (Cont)	PROGRAM LOAD rotary device select[3, 4] (Cont)	More significant octal digit determined by most significant PROGRAM TEST thumbwheel: 1X = address 10 or 11, IOE (operational) 4X = address 40 or 41, IOE 5X = address 50 or 51, IOE 6X = address 60 or 61, IOE 7X = address 70 or 71, IOX (system test) X = Don't care
25-31	(ACC ADDRESS)[2]	

[1] Used in AN/TSQ-73

[2] Used in TACFIRE

[3] Used in AN/TTC-39

[4] Used in NICS/TARE

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Section V. PERIPHERAL DEVICES

This section is subdivided to show the differences in peripheral devices that depend upon the application. The subsections to follow are applicable to:

a. TACFIRE.

b. AN/TSQ-73.

c. AN/TTC-39.

d. NICS-TARE.

NOTE

The page numbers of the following subsections employ a capital letter reflecting the specific system as indicated above.

Section VA. PERIPHERAL DEVICES (TACFIRE)

4-18A. Peripheral Device Addresses (TACFIRE)

The peripheral devices and peripheral device addresses used in TACFIRE are listed in table 4-VA-1. The table consists of two parts, which list the peripheral devices and addresses for Division and Battalion and for the Programming Support Center (PSC). The Battalion peripheral devices are a subset of the Division.

Table 4-VA-1 shows the typical connection of the peripheral devices to the Input Output Exchanger (IOXs) and the peripheral device addresses assigned by software. They can be changed by selection of the cabling and the DATA EXCHANGE CHANNEL SELECT rotary switches on the Input Output Unit (IOU), see figure 4-IIIA-3, as well as the address select switch on the peripheral device.

4-19A. Connectors (TACFIRE)

The peripheral devices are connected to the IOU. Figure 4-IIIA-3 shows the three I/O connectors (A, B, and C) that are associated with the three IOXs (A, B, C). The front panel shows the DATA EXCHANGE CHANNEL SELECT rotary switches that are associated with the three IOXs and the three connectors.

Table 4-VA-1. Peripheral Device Addresses (TACFIRE)

DIVISION AND BATTALION				
IOE/IOX	Address	Peripheral Device		Remarks
----	00-07	Special Addresses		See tables 4-2 & 4-13
IOX A	10	Spare		
	11	ARMM 1	Auxiliary Removable Media Memory 1	System Program Load
	12	DDT A	Digital Data Terminal A	Receive
	13	DDT A		Transmit
	14	DDT B		
	15	DDT B		
	16	DDT C		
	17	DDT C		
IOX B	20	DDT D		
	21	DDT D		
	22	DDT E		
	23	DDT E		
	24	C/D	Compose/Edit	Artillery Control Console (ACC)
	25	SA	Switch Assembly	
	26	RD	Receive Display	
	27	ELP 2	Electronic Line Printer 2	
IOX C	30	DDT F		
	31	DDT F		
	32	DPM	Digital Plotter Map	
	33	*ELP 1	Electronic Line Printer 1	*Division Only (Absent in Battalion)
	34	*DDT G		
	35	*DDT G		
	36	*ARMM 2	Auxiliary Removable Media Memory 2	
	37	*ETD	Electronic Tactical Display	

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Table 4-VA-1. Peripheral Device Addresses (TACFIRE) (Cont)

PROGRAMMING SUPPORT CENTER				
IOE/IOX	Address	Peripheral Device		Remarks
IOX A		SIU	System Interface Unit of Smart Peripheral System (SPS)	
	11		Bootstrap program load	
	16		Data Transfer	
	17		Control	
IOE		PEBU	Peripheral Equipment Buffer Unit	Replaced by SIU/SPS
	10	For bootstrap program load		
		Magnetic Tape 1		
	70	Magnetic Tape 1		
	71	Magnetic Tape 2		
	72	Magnetic Tape 3		
	73	Magnetic Tape 4		
	74	Card Reader		
	75	Card Punch		
	76	Line Printer		
	77	Typewriter		

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Section VB. PERIPHERAL DEVICES (AN/TSQ-73)

4-18B. Peripheral Device Addresses (AN/TSQ-73)

The peripheral devices and peripheral device addresses used in AN/TSQ-73 are listed in table 4-VB-1. The table consists of two parts, which list the peripheral devices and addresses for Battalion and for the Programming Support Center.

Some of the peripheral device addresses indicated by an asterisk (*) on a given IOX are switch selectable; the others are fixed. Table 4-VB-1 shows the peripheral device addresses assigned by software.

4-19B. Connectors (AN/TSQ-73)

The Automatic Data Processor (ADP) External Interface panel contains connectors. Figure 4-VB-1 shows the connector arrangement and table 4-VB-2 lists the functions at the connectors.

The memory port connectors when not in use, must be terminated with a terminator cap. Additional memories can be connected to the memory port connectors; in this case, the terminator caps must be placed at the cable end after the last added memory.

The Computer Test Set (CTS) or the System Control Console (SCC), used in a Programming Support Center (PSC) are connected to the upper CPU by the CTS and Memory Port B connectors. A second CTS or SCC can be connected to the lower CPU by the CTS and Memory Port C connectors.

Table 4-VB-1. Peripheral Device Addresses (AN/TSQ-73)

BATTALION AND GROUP				
IOX/IOE	Address	Peripheral Device		Remarks
-----	00-07	Special Addresses		See tables 4-2 & 4-13
IOX 1	10	*MTU 1	Magnetic Tape Unit 1 (REC/REP-Recorder Reproducer Set)	System Program Load
	11	*MTU 2	Magnetic Tape Unit 2	
	12	RIE	Radar Interface Equipment	Target Report Input
	13	VSU	Video Simulator Unit	
	14	*DDG *SDP	Data Display Group or Status Display Panel	
	15	RIE	Radar Interface Equipment	Control
	16	*DDG *SDP	Data Display Group or Status Display Panel	Only Group or Remote
	17	KPU	Keyboard Printer Unit	
IOX 2	20	*	Display Console 1	
	21	*	Display Console 2	
	22-27		(Display Console Expansion	Remote
IOE 10		IOM	Input Output Multiplexer	
	100		Modem 1	Input
	101		Modem 1	Output
	.		.	
	.		.	
	.		.	
	107		Modem 4	Output
IOE 11	110-117		Modems 5-8	Max Group
IOE 12	120-127		Modems 9-12	
IOE 13	130-137		Modems 13-18	Max Battalion
IOE 14	130-137		Modems 17-20	

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Table 4-VB-1. Peripheral Device Addresses (AN/TSQ-73) (Cont)

BATTALION AND GROUP (Cont)			
IOX/IOE	Address	Peripheral Device	Remarks
IOE 15	140-147	(Modems 21-24)	Expansion
.	.	.	
.	.	.	
.	.	.	
IOE 17	170-177	(Modems 29-32)	
PROGRAMMING SUPPORT CENTER			
IOE		PEBU Peripheral Equipment Buffer Unit	
	10	For bootstrap program load	
		Magnetic tape 1	
	70	Magnetic Tape 1	
	71	Magnetic Tape 2	
	72	Magnetic Tape 3	
	73	Magnetic Tape 4	
	74	Card Reader	
	75	Card Punch	
	76	Line Printer	
	77	Typewriter	
IOX 1		SIU System Interface Unit of Smart Peripheral System (SPS):	Replaces PEBU
	11	Bootstrap program load	
	16	Data transfer	
	17	Control	

NOTE: *Switch selectable

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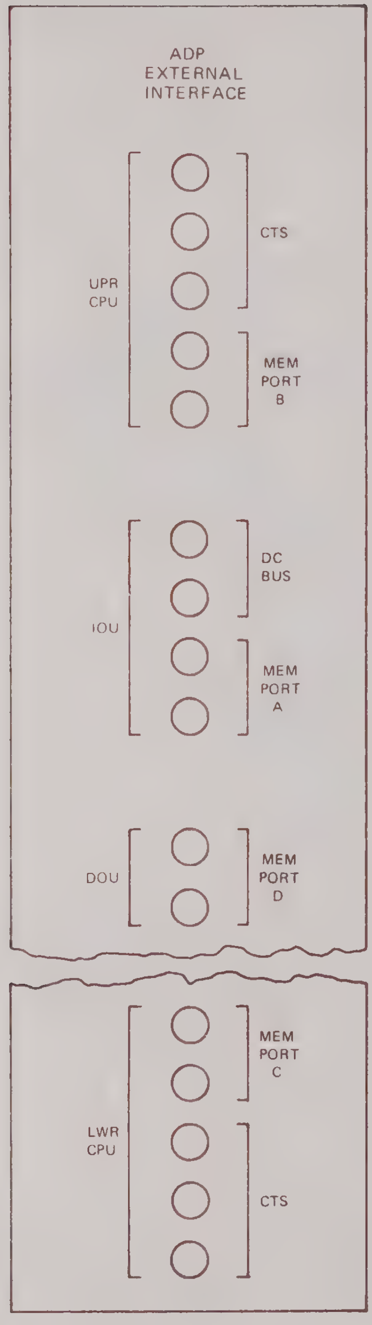
ADP
EXTERNAL
INTERFACE
CTS
UPR
CPU
MEM
PORT
B
DC
BUS
IOU
MEM
PORT
A
DOU
MEM
PORT
D
MEM
PORT
C
LWR
CPU
CTS

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Figure 4-VB-1. ADP External Interface Panel

Table 4-VB-2. Connector Functions on ADP External Interface Panel (AN/TSQ-73)

Connector	Description	Terminator	Remarks
UPR CPU CTS	Upper CPU Computer Test Set (or SCC-System Control Console)	No	First CTS or SCC for lower CPU
MEM PORT B	Memory Port B	Yes	
IOU DC BUS	Input Output Unit Internal I/O Bus	No	To connect System Interface Unit (SIU), Smart Peripheral System (SPS), or Peripheral Equipment Buffer Unit (PEBU)
MEM PORT A	Memory Port A	Yes	Highest Priority
DOU MEM PORT D	Display Output Unit Memory Port D	Yes	Lowest Priority
LWR CPU MEM PORT C	Lower CPU Memory Port C	Yes	
CTS	Computer Test Set		Second CTS on SCC for lower CPU

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Section VC. PERIPHERAL DEVICES (AN/TTC-39)

4-18C. Peripheral Device Addresses (AN/TTC-39)

The peripheral devices and peripheral device addresses used in AN/TTC-39 are listed in table 4-VC-1. The table consists of two parts, which list the peripheral devices and addresses for the Message Switch and for the Circuit Switch separately.

The peripheral device addresses are wired-in and are not switch selectable.

Table 4-VC-1. Peripheral Device Addresses (AN/TTC-39)

IOE/IOX	Address	Peripheral Device	Remarks
---	00-07	Special Addresses	See tables 4-2 & 4-13
IOE 1	10	MTC A Magnetic Tape Controller A	System Program Load
	11	MTC B Magnetic Tape Controller B	
	12	MTC C Magnetic Tape Controller C	
	13	MTC D Magnetic Tape Controller D	
	14	RASC A Random Access Storage Cont. A	
	15	RASC B Random Access Storage Cont. B	
	16	LP A Line Printer A	
	17	LP C Line Printer C	
IOE 2	20	LP B Line Printer B	
	21	TTY Teletypewriter	
	22	Reserved	GTE/Delco
	23	VDU A Visual Display Unit A	
	24	VDU B Visual Display Unit B	
	25	VDU C Visual Display Unit C	
	26	Reserved	GTE
	27	Reserved	GTE
IOE 3	30	CIP Control Interface Processor	GTE/Delco
	31	↕	↕
	32		
	33		
	34		
	35		
	36		
	37	CIP Control Interface Processor	GTE/Delco

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Table 4-VC-1. Peripheral Device Addresses (AN/TTC-39) (Cont)

IOE/IOX	Address	Peripheral Device	Remarks
---	00-07	Special Addresses	See tables 4-2 & 4-13
IOE 1	10	MTC Magnetic Tape Controller	System Program Load
	11-13	Spares	
	14	TTY A Teletypewriter A	
	15	VDU Visual Display Unit	
	16	PPI Processor to Processor Interface	
	17	TTY B Teletypewriter B	
IOX 3	30	Reserved	GTE
	31		
	32		
	33		
	34		
	35		
	36		
	37	Reserved	GTE
IOE 4	40	Reserved	GTE
	41		
	42		
	43		
	44		
	45		
	46		
	47	Reserved	GTE

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4-18D. Peripheral Device Addresses (NICS-TARE)

The peripheral devices and peripheral device addresses used in NICS-TARE are listed in table 4-VD-1.

The peripheral device addresses are wired-in and are not switch selectable.

4-19D. Connectors (NICS-TARE)

The lower portion of each of the two Automatic Data Processor (ADP) Status and Control Panel contains connectors. Figure 4-VD-1 shows the connector arrangement and table 4-VD-2 lists the functions of the connectors. Other connectors are located on the Peripheral Interface Panel (PIP) inside the cabinet.

The Port and IOE connectors, when not in use, must be terminated with a terminator cap. Additional memories and peripheral devices can be connected to the Port and IOE connectors; in this case, the terminator caps must be placed at the end of the cable after the last added memory and peripheral device.

The System Control Console (SCC), used in a Programming Support Center (PSC), is connected to the SCC and PORT D CPU connectors.

Table 4-VD-1. Peripheral Device Addresses (NICS-TARE)

IOE/IOX	Address	Peripheral Device	Remarks
---	00-07	Special Addresses	See tables 4-2 & 4-13
IOE 1	10	Disc A	System Program Load
	11	Disc B	System Program Load
	12-17	Spares	
IOE 2	20-27	Spares	Card but no connector
---	30-37	Not implemented	
IOE 4	40	VDU Visual Display Unit	9600 Baud
	41	VDU Visual Display Unit	9600 Baud
	42	RSD Remote Status Display	9600 baud
	43	RTP Report Teleprinter	300 baud
	44	JBR Journal Balance Recorder (Floppy Disc)	9600 Baud
	45,46	Spares	
	47	Secondary processor to processor interface	Software-selectable Baud rate
IOE 5	50	VDU Visual Display Unit	9600 Baud
	51	VDU Visual Display Unit	9600 Baud
	52	VDU (Expansion)	
	53	RTP Report Teleprinter	300 Baud
	54	JBR Journal Balance Recorder (Floppy Disc)	9600 Baud
	55,56	Spares	
	57	Secondary Processor to Processor interface	Software-selectable Baud rate

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Table 4-VD-1. Peripheral Device Addresses (NICS-TARE) (Cont)

IOE/IOX	Address	Peripheral Device	Remarks
IOE 6	60	VDU Visual Display Unit	9600 Baud
	61	VDU Visual Display Unit	9600 Baud
	62	RQP Report Queue Punch	1200 Baud
	63	CLT Command Log Teleprinter	300 Baud
	64-67	Spares	
IOX 7	70	CP A Communications Processor A	
	71	CP B Communications Processor B	
	72	PPI Processor to Processor Interface	Combined with ESCC
	73	ESCC Equipment Status and Configuration Control (Panel)	
	74-77	Spares	

NOTE: IOE 4, 5, 6 are located on Internal Channel Controller (ICC) of Interface Control Unit (IFCU).

70061-72-2

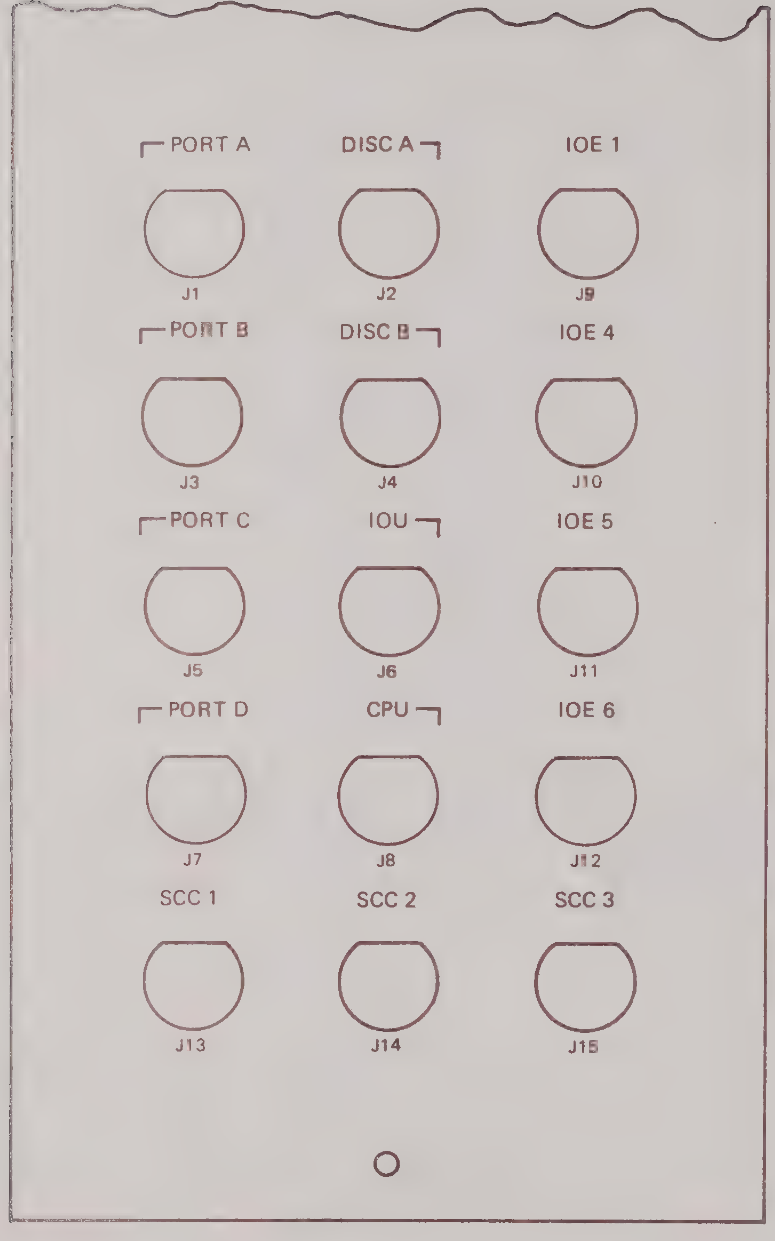
PORT A
DISC A
IOE 1
J1
J2
J9
PORT B
DISC B
IOE 4
J3
J4
J10
PORT C
IOU
IOE 5
J5
J6
J11
PORT D
CPU
IOE 6
J7
J8
J12
SCC 1
SCC 2
SCC 3
J13
J14
J15

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Figure 4-VD-1. Connector Portion of ADP Status and Control Panel (NICS-TARE)

Table 4-VD-2. Connector Functions on Connector Portion of ADP Status and Control Panel (NICS-TARE)

Connector	Description	Terminator	Remarks
PORT A DISC A	Memory Port for Disc A	Yes	Highest Priority
PORT B DISC B	Memory Port for Disc B	Yes	
PORT C IOU	Memory Port for IOU	Yes	
PORT D CPU	Memory Port for CPU	Yes	Lowest Priority
IOE 1	Input Output Expander	Yes	See table 4-VD-1
IOE 4		Yes	
IOE 5		Yes	
IOE 6		Yes	
SCC 1	System Control Console	No	SCC is connected to SCC 1, SCC 2, SCC 3, and Port D
SCC 2		No	
SCC 3		No	

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CHAPTER 5

DATA AND INSTRUCTIONS

Section I. DATA WORD FORMAT

5-1. Introduction

This chapter provides information pertaining to the computer data word and instruction word format. Formats representing data and instruction words are presented and explained.

5-2. Data

The programmer may select data words of a single bit, a 'byte' of eight bits, a half-word of 16 bits, a word of 32 bits and, on some instructions, a double word of 64 bits (see figure 5-1). Within limits, the data word size is a function of the programmer's option on the instruction to be executed. On arithmetic and logical instructions, either half word or word operations are allowed. Special instructions are provided for test and modification of single bits within a half word. Special byte handling instructions are also provided. Double-word products are generated on multiply instructions; double-word dividends are used in divide instructions; and double-word register pairs are allowed in shift instructions. Memory addresses are considered as half-word addresses because the operand address field of the instruction word contains a single bit (in bit position 31) called the W field. This bit will select either the leftmost 16 bits of a selected word if it is ZERO (W = 0), or it will select the right-most 16 bits of a selected word if it is ONE (W = 1). Therefore, all word addresses are even numbers. On word operations, the W bit of the instruction is ignored, and the address is treated as an even number. Bytes of eight bits are selected on half-word instructions as either the upper byte or lower byte by the operation code of the instruction. Single bit positions of a half-word are selected by use of the H field of the instruction word. Double words must be located in memory with a half-word address that is evenly divisible by four. Whenever double words are addressed, the least significant two bits of the address are assumed to be ZEROS. The storage of partial words and double words within memory is shown in the illustration defining integral boundaries for data formats (figure 5-1). A data word may contain a numerical or logical quantity. Numerical quantities are treated as signed integers. Logical quantities include unsigned numbers (e.g., addresses) or collections of individual bits and fields.

a. *Numerical Word Formats.* The computer is capable of operating on half-words, full words, and double words as shown in figures 5-2, 5-3, and 5-4, respectively. Numerical words have the following characteristics:

(1) Half words contain 16 bits, full words contain 32 bits, and double words contain 64 bits.

(2) Numbers are processed as binary integers with negative numbers in two's complement form.

(3) Bit positions are assigned sequentially, left to right, with the most significant bit (MSB) in the leftmost position.

(4) The sign bit (S) is ZERO for positive numbers and ONE for negative numbers and is located at the most significant bit position of the data.

b. *Two's Complement Arithmetic Notation.* Arithmetic operations within the computer process numbers as binary integers in two's complement form. Two's complement form differs from one's complement only in negative number representations. In a 16 bit half word, positive values have a range of +0 to $+32{,}767_{10}$. This includes a sign bit (always ZERO for positive values) and fifteen magnitude bits to represent the value. The range is the same for both one's and two's complement form.

(1) In one's complement form (for reference only), negative values for the same 16 bit half word have a range of –0 to $-32{,}767_{10}$. This includes a sign bit (always ONE for negative numbers) and fifteen magnitude bits to express the value. To find the one's complement of a value all that is required is the changing of ONE bits to ZERO bits and ZERO bits to ONE bits in the binary notation.

EXAMPLE: $+200_{10} = 0000000011001000_2$

To obtain the one's complement of the above value merely change the ZERO bits in the binary notation to ONE bits and the ONE bits to ZERO bits. Thus:

$-200_{10} = 1111111100110111_2$

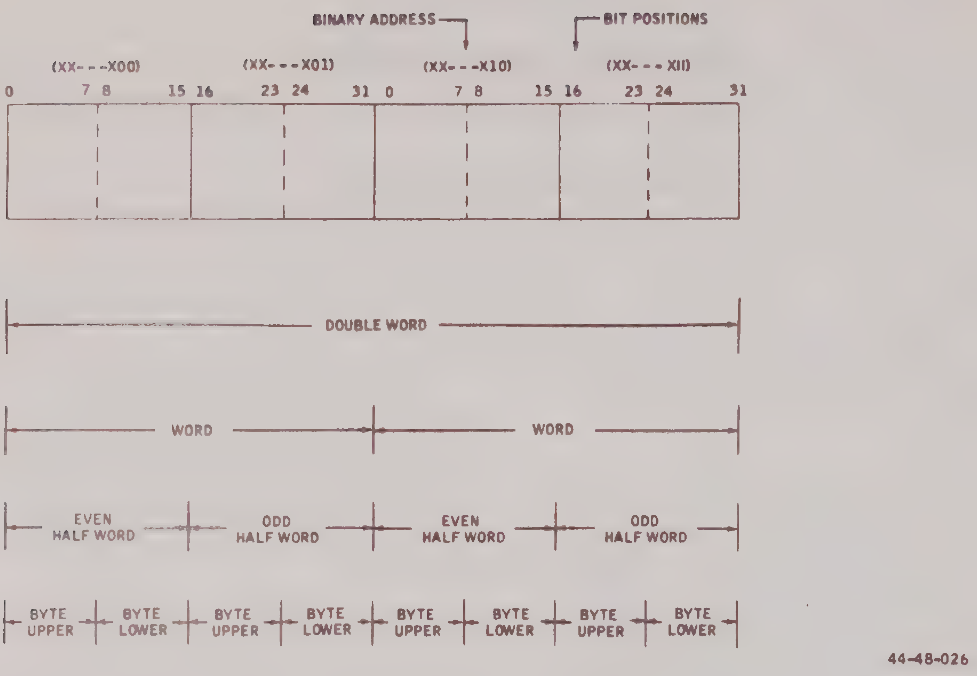
BINARY ADDRESS
BIT POSITIONS
(XX- - -X00)
(XX- - -X01)
(XX- - -X10)
(XX- - - XII)
0 7 8 15 16 23 24 31 0 7 8 15 16 23 24 31
DOUBLE WORD
WORD
WORD
EVEN HALF WORD
ODD HALF WORD
EVEN HALF WORD
ODD HALF WORD
BYTE UPPER
BYTE LOWER
BYTE UPPER
BYTE LOWER
BYTE UPPER
BYTE LOWER
BYTE UPPER
BYTE LOWER
44-48-026

Figure 5-1. Integral Boundaries for Data Formats

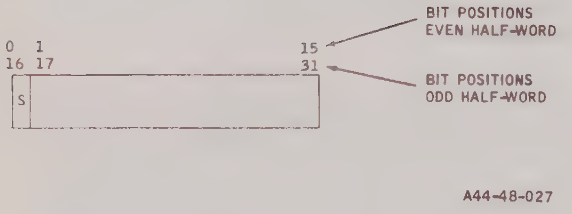
BIT POSITIONS
EVEN HALF-WORD
BIT POSITIONS
ODD HALF-WORD
0 1
16 17
15
31
S
A44-48-027

Figure 5-2. Numerical Half Word Format — 16 Bits

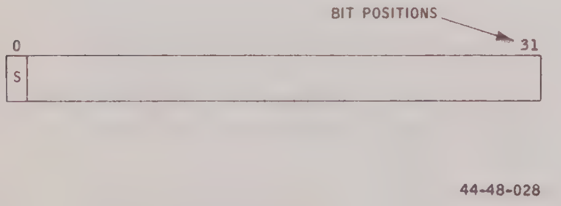
BIT POSITIONS
0
31
S
44-48-028

Figure 5-3. Numerical Word Format — 32 Bits

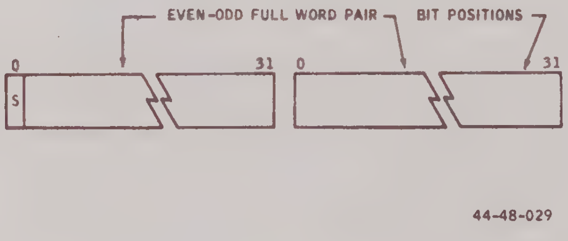
EVEN-ODD FULL WORD PAIR
BIT POSITIONS
0
31
0
31
S
44-48-029

Figure 5-4. Numerical Double Word Format — 64 Bits

(2) In two's complement form, negative values for a 16 bit half word have a range of −1 to $-32{,}768_{10}$. This includes a sign bit and fifteen magnitude bits to express the value. Notice there is no negative ZERO. A word of all ONE bits represents minus one. Since there is no negative ZERO, the largest possible negative number ($-32{,}768_{10}$) equals -2^{15}, one greater than the complement of the largest possible positive number ($+32{,}767_{10}$), $+2^{15} -1$. To obtain the two's complement of a binary number, invert each bit within the number (as in one's complement) and add one to the low order (least significant) bit position.

EXAMPLE: $+200_{10} = 0000000011001000_2$

One's Complement $-200_{10} = 1111111100110111_2$

$$\underline{\qquad\qquad\qquad\qquad 1}$$

Two's Complement $-200_{10} = 1111111100111000_2$

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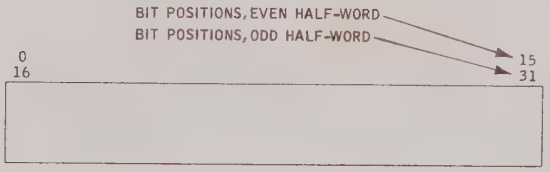
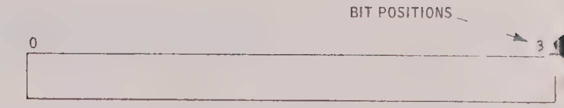
In a 32 bit word the largest possible negative number is -2^{31} ($-2,147,483,648_{10}$). The largest possible positive number is $+2^{31} - 1$ ($+2,147,483,647_{10}$).

c. *Logical Word Formats.* The computer is capable of performing logical operations on data in the form of full words, half words, and eight-bit quantities (bytes). Figures 5-5 and 5-6 represent the logical word formats and figures 5-7 and 5-8 represent the byte positions in each half word.


BIT POSITIONS, EVEN HALF-WORD
BIT POSITIONS, ODD HALF-WORD
0
16
15
31

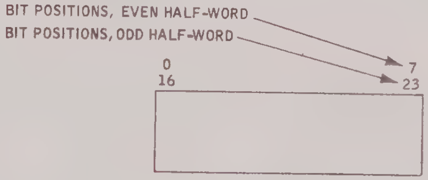
44-48-030

Figure 5-5. Logical Half Word Format — 16 Bits


BIT POSITIONS
0
3

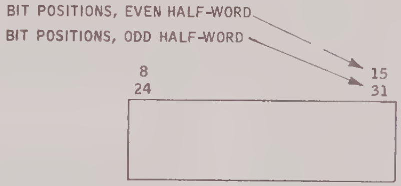
44-48-031

Figure 5-6. Logical Word Format — 32 Bits


BIT POSITIONS, EVEN HALF-WORD
BIT POSITIONS, ODD HALF-WORD
0
16
7
23

44-48-032

Figure 5-7. Upper Byte Position — 8 Bits


BIT POSITIONS, EVEN HALF-WORD
BIT POSITIONS, ODD HALF-WORD
8
24
15
31

44-48-033

Figure 5-8. Lower Byte Position — 8 Bits

Section II. INSTRUCTION WORD FORMAT

5-3. Introduction

The computer uses a 32-bit instruction word with the format shown in figure 5-9. The normal use and definition of each instruction word field is provided in the subsequent paragraphs. Special uses made of an instruction field are as specified in the descriptions of the instructions.

a. *E, Operand Size, Bit Position 0.* This one-bit field generally specifies a 16-bit half word operation or a 32-bit word operation; $E = 0$ – full word operation, $E = 1$ – half word operation.

b. *F, Operation, Bit Positions 1 to 6.* This six-bit field specifies the basic operation to be performed by the instruction. The E and F fields together represent the Function Code.

c. *M, Addressing Mode, Bit Positions 7 and 8.* This two-bit field provides four basic addressing modes, literal, direct, relative, and indirect; which are expanded to nine modes according to the S-field value.

d. *H, Accumulator, Bit Positions 9 to 12.* This four-bit field selects one of 16 process registers to be used as an accumulator.

e. *S, Index, Bit Positions 13 to 15.* This three-bit field selects one of seven, 16-bit process registers to be used for operand address indexing. These process registers are also addressable as accumulators with the H-field. $S = 0$ defines the nonindexed addressing modes.

f. *CA, Operand Address, Bit Positions 16 to 31.* The operand address field, CA, is a 16-bit field that is either an operand itself in the literal address modes, a special address (refer to paragraph 5-3f(1) below) or a memory address, in which case, it is divided into three subfields, D, A, and W (refer to paragraphs 5-3f(2) thru 5-3f(4) below).

(1) Special Addresses. For final operand or transfer addresses in the range of 0000 to $0003F_{16}$, the operand is located in selected registers as indicated in table 5-1 and described in Section 3. Privilege status is required to modify registers selected by the special addresses as indicated in table 5-1.

(2) D, Page, Bit Positions 16 to 19. This four-bit field selects one of 16 page control and address registers.

(3) A, Word Address, Bit Positions 20 to 30. These 11 bits select one of 2048 words within a page selected by the page address.

(4) W, Half Word Address, Bit Position 31. This bit is used in half word operations to select the most significant 16 bits or the 16 least significant bits of a 32-bit word as an operand. Even address, $W = 0$, selects bits 0 to 15 of the memory word or special address register. Odd address, $W = 1$, selects bits 16 to 31 of the memory word or special address register. In full word operations this bit is assumed to be ZERO and its setting is ignored.

5-4. Address Modes

The M field and S field in the instruction are used to select address mode. These modes are defined as follows:

a. *M = 0, S = 0 – Literal.* The operand address field of the instruction is used as a 16-bit operand. No memory cycle is required to obtain an operand. It is possible to use this half word as an operand, a transfer address, a format instruction, a shift instruction, or an input/output instruction. Using this mode with full-word accumulators, the half word is assumed to be right-justified with the sign bit extended 16 bits to the left or ZERO extended depending upon the instruction.

b. *M = 0, S = 1 to 7 – Literal with Indexing.* The operand address field of the instructions is used as a 16-bit operand as specified in paragraph 5-3a, except that the contents of the process register selected by the S field are added algebraically to this 16-bit quantity initially. Overflow is detected on this addition for algebraic instructions.

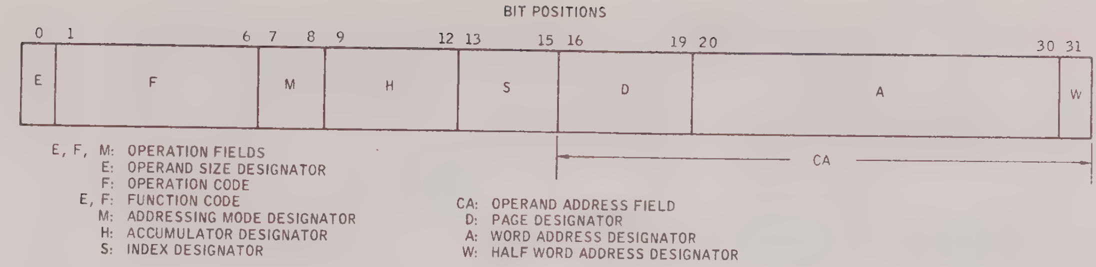
c. *M = 1, S = 0, Direct.* The CA field of the instruction word directly specifies an operand address. On transfer instructions or full 32-bit operand addresses, W is assumed to be ZERO.

d. *M = 1, S = 1 to 7 – Direct with Indexing.* The operand address field of the instruction is added as an unsigned 16-bit quantity to the contents of the process register (index) that is selected by the S field. Overflow on this addition is discarded. The sum is used as the new operand address as in the direct mode.

e. *M = 2, S = 0 – Relative.* The relative address mode causes the contents of the instruction location register to be added unsigned to the operand address of the instruction. Overflow on this addition is discarded and an operand address that is relatively located with respect to the next instruction in normal sequence results.

f. *M = 2, S = 1 – Relative with Indexing.* The operand address field of the instruction is added to the contents of process register (index) one and this 16-bit sum is added to the contents of the 16-bit instruction location register. This final sum is used as the operand address. Overflow on these unsigned additions is discarded.

g. *M = 2, S = 2 to 7 – Direct with Double Indexing.* The operand address field of the instruction is


BIT POSITIONS
0
1
6
7
8
9
12
13
15
16
19
20
30
31
E
F
M
H
S
D
A
W
CA
E, F, M: OPERATION FIELDS
E: OPERAND SIZE DESIGNATOR
F: OPERATION CODE
E, F: FUNCTION CODE
M: ADDRESSING MODE DESIGNATOR
H: ACCUMULATOR DESIGNATOR
S: INDEX DESIGNATOR
CA: OPERAND ADDRESS FIELD
D: PAGE DESIGNATOR
A: WORD ADDRESS DESIGNATOR
W: HALF WORD ADDRESS DESIGNATOR

63-1-007

Figure 5-9. Instruction Word Format

Table 5-1. Special Operand Addresses

Special Address (Hex)	Register Selected	Privilege Status
0000 – 001F	Active process registers	Not required
0020 – 002F	Active page control and address registers	Required
0030 – 0031	Privilege and level link register	Required
0032 – 0033	Queue register	Not required
0034 – 0035	Query register	Required
0036	Executive link register	Required
0037	Unused	Required
0038 – 003F	Program activity registers	Required

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added to the contents of process register (index) one. This 16-bit sum is added to the contents of the process register (index) that is selected by the S field of the instruction and this final sum is used as the operand address. Overflow on these unsigned additions is discarded.

h. *M = 3, S = 0 – Indirect.* The CA field specifies a half word location. The contents of this half word location specifies the address of the operand.

i. *M = 3, S = 1 to 7 – Indirect, Indexed.* The CA field specifies a half word location. The contents of this half word location is added to the contents of the process register (index) specified by the S field. The sum specifies the address of the operand. Overflow on this unsigned addition is discarded. The possible operand and transfer addresses that can be generated with the nine modes are summarized in table 5-2.

5-5. Instruction Execution Times

The nominal execution times for the instruction set described in chapter 6 applies for the direct addressing mode and when there is no conflict for use of a memory bank due to an I/O data transfer. Execution times will vary with specific conditions as follows:

a. Instruction execution time will be increased by not more than the following specified times:

(1) 0.8 microsecond when using the indexed address mode.

(2) 0.8 microsecond when using the relative address mode.

(3) 2.5 microseconds when using the indirect address mode.

(4) The time required to complete the I/O data transfer which requires the use of the same memory bank as the instruction.

b. Instruction execution times will be decreased by more than 0.9 microsecond when using the literal addressing modes and operands which address process registers.

Table 5-2. Data Operand and Transfer Instruction Addresses

Mode			Action			
M-Field	S-Field	Name	Operand Address	Indirect Operand Address	Operand	Transfer Instruction Address
0	0	Literal			CA = Z	CA = Z*
0	1-7	Literal indexed			CA + (S) = Z	CA + (S) = Z*
1	0	Direct	CA = Y		(Y) = Z	(Y) = Z*
1	1-7	Direct indexed	CA + (S) = Y		(Y) = Z	(Y) = Z*
2	0	Relative	CA + ILR = Y		(Y) = Z	Y = Z*
2	1	Relative indexed	CA + ILR + (S=1) = Y		(Y) = Z	Y = Z*
2	2-7	Direct double indexed	CA + (S=1) + (S) = Y		(Y) = Z	Y = Z*
3	0	Indirect	CA = X	(X) = Y	(Y) = Z	(Y) = Z*
3	1-7	Indirect indexed	CA = X	(X) + (S) = Y	(Y) = Z	(Y) = Z*

NOTES:

CA: Instruction address field

ILR: Instruction location register

M: Mode designator

S: Index designator

X: Indirect operand address

Y: Direct operand address

Z: Operand

Z*: Transfer address

( ): Contents of

5-6. Instruction Functions

Table 5-3 is a list of the major functions for the instructions arranged by classes. The definition of the columns and the symbols used in the columns are as follows:

a. *Modes*: Refers to the addressing modes.

Xfer = Transfer Instruction Address applicable
Operand = Operand applicable
0 excluded = Mode 0 is excluded
Other = Other addressing mode
X = Applicable
# = See instruction description

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b. *Special Addresses*: Refers to addresses in the range of 0000 to $003F_{16}$.

N/A = Not Applicable
PR only = Process Registers only
PR = Process Registers
PCA = Page Control and Address registers
PLL = Privilege and Level Link register
Queue = Queue register
Query = Query register
EXL = Executive Link register
PAR = Program Activity registers
X = Applicable
P = Privilege required
S = Semiprivilege or privilege required
# = See instruction description
P = See instruction description, privilege required

70061-1003

c. *Indicators*:

CF = Carry Flag
OF = Overflow/greater flag
EF = Equal/excess flag
LF = Less flag
Other = See instruction description
X = Affected
– = Not affected
R = Reset
L = May be set by Mode 0

70061-1004

d. *Trap*

X = Trap on overflow occurs when OT indicator is ZERO
R = Trap never occurs
i = Trap on overflow occurs only in Mode 0 with indexing and only when OT indicator is ZERO
# = See instruction description

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Table 5-3. Inst[illegible]n Functions

Mnemonic	Name	Modes				Special Addresses									Indicators					Trap
		Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	
DATA HANDLING INSTRUCTIONS																				
E X F	Exchange Full			X				X	#P	P	X	#P	P	P	R	R	X	R	–	R
E X H	Exchange Half			X			X								R	R	X	R	–	R
L A F	Load Absolute Full		X				X								i	X	X	R	–	X
L A H	Load Absolute Full		X				X								i	X	X	R	–	X
L C F	Load Two's Complement Full		X				X								i	X	X	R	–	X
L C H	Load Two's Complement Half		X				X								i	X	X	R	–	X
L D F	Load Full		X					X	#	X	X	#	X	X	i	i	i	R	–	i
L D H	Load Half		X					X	#	X	X	#	X	X	i	i	i	R	–	i
L D L	Load from Lower Byte		X				X								i	i	i	R	–	i
L D U	Load from Upper Byte		X				X								i	i	i	R	–	i
L M H	Load Most Half		X				X								i	i	i	R	–	i
M I L	Move Into Lower Byte				#			X	#P	P	X	#P	P	P	–	–	–	–	–	R
M I U	Move Into Upper Byte				#			X	#P	P	X	#P	P	P	–	–	–	–	–	R
M Z F	Move All Zeroes Full			X				X	#P	P	X	#P	P	P	–	–	–	–	–	R
M Z H	Move All Zeroes Half			X				X	#P	P	X	#P	P	P	–	–	–	–	–	R
S D F	Store Full			X				X	#P	P	X	#P	P	P	R	R	X	R	–	R
S D H	Store Half			X				X	#P	P	X	#P	P	P	R	R	X	R	–	R
S D L	Store Into Lower Byte			X			X								–	–	–	–	–	R
S D U	Store Into Upper Byte			X			X								–	–	–	–	–	R
S M H	Store Most Half			X				X	#P	P	X	#P	P	P	–	–	–	–	–	R

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Table 5-3. Instruction Functions (Cont)

Mnemonic	Name	Modes				Special Addresses									Indicators					Trap
		Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	
ARITHMETIC INSTRUCTIONS																				
A D F	Add Full		X				X								X	X	X	R	–	X
A D H	Add Half		X				X								X	X	X	R	–	X
A L F	Add Logical Full		X				X								X	X	X	R	–	R
A L H	Add Logical Half		X				X								X	X	X	R	–	R
D I F	Divide Full		X				X								i	X	X	R	–	X
D I H	Divide Half		X				X								i	X	X	R	–	X
M P F	Multiply Full		X				X								X	X	X	R	–	X
M P H	Multiply Half		X				X								X	X	X	R	–	X
R A F	Replace Add Full			X			X								X	X	X	R	–	X
R A H	Replace Add Half			X			X								X	X	X	R	–	X
R Q F	Replace Square Root Full			X			X								R	X	X	R	–	X
R S F	Replace Subtract Full			X			X								X	X	X	R	–	X
R S H	Replace Subtract Half			X			X								X	X	X	R	–	X
S B F	Subtract Full		X				X								X	X	X	R	–	X
S B H	Subtract Half		X				X								X	X	X	R	–	X
S L F	Subtract Logical Full		X				X								X	X	X	R	–	R
S L H	Subtract Logical Half		X				X								X	X	X	R	–	R

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Table 5-3. Instruction Functions (Cont)

Mnemonic	Name	Modes				Special Addresses									Indicators					Trap
		Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	
TRANSFER INSTRUCTIONS																				
X D O	Test, Conditionally Decrement by One and Transfer	X					X													R
X D T	Test, Conditionally Decrement by Two and Transfer	X					X									–		–	–	R
X E F	Transfer if Process Register is Zero	X					X								–		–	–	–	R
X E X	Execute	X					X								–	–	–	–	–	R
X F R	Transfer Unconditionally	X					X								–	–	–	–	–	R
X I N	Transfer On Indicators	X					X								–	–	–	–	–	R
X I O	Test, Conditionally Increment by One and Transfer	X					X								–	–	–	–	–	R
X I T	Test, Conditionally Increment by Two and Transfer	X					X								–	–	–	–	–	R
X L K	Transfer and Store Link	X					X								–	–	–	–	–	R
X N F	Transfer if Process Register is Negative	X					X								–	–	–	–	–	R
X P F	Transfer if Process Register is Positive	X					X								–	–	–	–	–	R
X S W	Transfer on Test Switches	X					X								–	–	–	–	–	R
X U F	Transfer if Process Register is not Zero	X					X								–	–	–	–	–	R

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Table 5-3. Instruction Functions (Cont)

		Modes				Special Addresses									Indicators					Trap
Mnemonic	Name	Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	
SHIFT INSTRUCTIONS																				
S H F	Shift Full (or Double)		X				X								i	i	i	R	–	R
S H H	Shift Half		X				X								i	i	i	R	–	R
COMPARE INSTRUCTIONS																				
C G F	Compare Gated Full		X				X								i	X	X	X	–	R
C G H	Compare Gated Half		X				X								i	X	X	X	–	R
C L F	Compare Logical Full		X				X								i	X	X	X	–	R
C L H	Compare Logical Half		X				X								i	X	X	X	–	R
C L L	Compare Logical Lower Byte		X				X								i	X	X	X	–	R
C L U	Compare Logical Upper Byte		X				X								i	X	X	X	–	R
C M F	Compare Algebraic Full		X				X								i	X	X	X	–	R
C M H	Compare Algebraic Half		X				X								i	X	X	X	–	R
C S F	Compare Selective Full		X				X								i	X	X	X	–	R
C S H	Compare Selective Half		X				X								i	X	X	X	–	R
M T H	Modify and Test Half			X			X								X	X	X	X	–	X

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Table 5-3. Instruction Functions (Cont)

		Modes				Special Addresses									Indicators					
Mnemonic	Name	Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	Trap
LOGIC INSTRUCTIONS																				
A N F	Logical AND Full		X				X								–	–	–	R		R
A N H	Logical AND Half		X				X								–	–	–	R	–	R
E O F	Exclusive OR Full		X				X								–	–	–	R	–	R
E O H	Exclusive OR Half		X				X								–	–	–	R	–	R
I O F	Inclusive OR Full		X				X								–	–	–	R		R
I O H	Inclusive OR Half		X				X								–	–	–	R	–	R
R E F	Replace Exclusive OR Full			X			X									–				R
R E H	Replace Exclusive OR Half			X			X									–				R
R I F	Replace Inclusive OR Full			X			X								–			–	–	R
R I H	Replace Inclusive OR Half			X			X								–	–	–	–	–	R
R N F	Replace Logical AND Full			X			X								–	–	–	–	–	R
R N H	Replace Logical AND Half			X			X								–			–	–	R
S S F	Selective Substitute Full			X			X								–	–	–	–	–	R

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Table 5-3. Instruction Functions (Cont)

		Modes				Special Addresses									Indicators					
Mnemonic	Name	Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	Trap
BIT INSTRUCTIONS																				
R B T	Reset Bit in Half Word			X				X	#P	P	X	#P	P	P	–	–	–	–	–	R
S B T	Set Bit in Half Word			X				X	#P	P	X	#P	P	P	–	–	–	–	–	R
T S I	Test and Conditionally Insert/Skip			X			X								–	–	–	–	–	R
T S O	Test Bit in Half Word for One, Skip on Match			X				X	#	X	X	#	X	X	–	–	–	–	–	R
T S Z	Test Bit in Half Word for Zero, skip on Match			X				X	#	X	X	#	X	X	–	–	–	–	–	R
FORMAT INSTRUCTIONS																				
F E F	Format Extract Full		X				X								i	i	i	R	–	R
F E H	Format Extract Half		X				X								i	i	i	R	–	R
F I F	Format Insert Full		X				X								i	i	i	R	–	R
F I H	Format Insert Half		X				X								i	i	i	R	–	R
PROGRAM LEVEL TRANSFER INSTRUCTIONS																				
T C P	Call Program Level and Link		X					X							–	–	–	–	–	R
T I L	Tie Program Level and Link		X					S											–	R
T Q R	Test and Conditionally Reset/Skip			X				X			X					–	–	–	–	R
T X P	Call Executive Program Level and Link		X					X							–		–		–	R

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Table 5-3. Instructi– [illegible]unctions (Cont)

Mnemonic	Name	Modes				Special Addresses									Indicators					Trap
		Xfr	Operand	0 Excluded	Other	N/A	PR Only	PR	PCA	PLL	Queue	Query	EXL	PAR	CF	OF	EF	LF	Other	
INPUT/OUTPUT INSTRUCTIONS																				
D E V	Device Command		X				P												#	R
D E X	Device Command and Exit		X				P								–			–	#	R
I T R	Input to Register		X				P										–		#	R
O F R	Output from Register		X				P									–	–	–	#	R
MISCELLANEOUS INSTRUCTIONS																				
D I G	Diagnose				#	X														R
H L T	Conditional Halt		X				X									–		–	–	R
L L O	Level Lock Set		X			X									–	–	–	–	–	R
L L R	Level Lock Reset		X			X									–		–		–	R
L O D	Load Call Destination		X			X													–	R
M B A	Memory Bank Assignment or Test		X				X								–	–	–	–	#	R
N O I	No Operation		X			X												–		R
T R I	Trap Instructions (Unused Codes)		X			X									–				#	#

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CHAPTER 6

INSTRUCTION DESCRIPTIONS

Section I. INTRODUCTION

6-1. General

This chapter presents detailed information about the operation of the instructions of the computer. Detailed information, along with coding examples, is provided for each of the instructions. Additional information concerning the operation of the input/output instructions can be found in chapter 4.

Instruction timings given in this chapter apply for the computer with memories of 2.0 microsecond cycle time. Instruction times for other memory cycle times are given in Appendix A. The introduction to Appendix A lists the memories, memory cycle times, and the applications. The instructions are listed by classes as follows:

a. *Data Handling Instructions.*
   (1) Load register instructions.
   (2) Store register instructions.
   (3) Move instructions.
   (4) Exchange instructions.
b. *Arithmetic Instructions.*
   (1) Fixed Point Arithmetic Instructions
c. *Transfer Instructions.*
   (1) Control transfer instructions.
   (2) Index test instructions.
   (3) Process register test instructions.
d. *Shift Instructions.*
e. *Compare Instructions.*
f. *Logic Instructions.*
g. *Bit Instructions.*
h. *Format Instructions.*
i. *Program Level Transfer Instructions.*
j. *Input/Output Instructions.*
k. *Miscellaneous Instructions.*

6-2. Instruction Notation

Certain symbols and notations are used frequently in the subsequent definitions of the instructions. Table 6-1 specifies the symbols used and their corresponding definitions. Table 6-2 contains definitions of notes frequently used in the instruction descriptions.

6-3. General Information

In the following instruction descriptions it is assumed that all addressing modes are permitted with the given instruction unless otherwise stated. The instruction times shown for the computer assume direct mode (mode 1) with no operand in the base page of memory. In all computer instructions a process register may be used in the operand of the instruction. Therefore it is possible to load or add one register to another. This is accomplished by using the address 0 – 15 as the contents of the operand field. This will access the process registers for the active program level. Therefore the only method that can be used to access absolute locations 0 – 15 in memory is to specify these locations through the page control and address registers or by using the execute (XEX) instruction.

Section II. DATA HANDLING INSTRUCTIONS

6-4. General

The data handling instructions are those instructions which transmit words or bits of data from one location to another. The several categories of transmissive instructions are presented below.

6-5. Load (Register) Instructions

The following paragraphs describe the load instructions.

a. *Load Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) replaces

Table 6-1. Instruction Symbols

Symbol	Definition
H	The four-bit field of an instruction word which generally references a process register
H_e	The reference to an even number process register by the instruction's H field
H_o	The reference to an odd numbered process register by the instruction's H field
R_{14}	The reference to process register 14 by the instruction's H field
R_{15}	The reference to process register 15 by the instruction's H field
ILR	The designation for the instruction location register
	NOTE Contains the address of the next instructions in sequence except when modified by the current instructions.
Y	The general representation for the instruction's effective operand address
Z^*	The general representation for a transfer address
$(\quad)$	The representation for the contents of the register or memory location that is referenced by the quantity within the parentheses
$(\quad)_{m-n}$	The field representation for the contents of a field of the designated register or memory location. Subscripts m and n specify the left and right boundaries of the field, respectively
$(Y)_U$	The representation for the contents of the upper byte of the memory half word addressed by Y
$(Y)_L$	The representation for the contents of the lower byte of the memory half word addressed by Y
$(\quad)_S$	The representation for the contents of a sign extended, 16-bit designated quantity
$(\quad)_i$	The representation for the contents of the ith bit position of the designated quantity
$\overline{(\quad)}$	The representation for the one's complement of the contents of the designated quantity
$\|\|$	The symbol designating the absolute value
$\vee$	The symbol designating the logical operation of inclusive OR
$\forall$	The symbol designating the logical operation of exclusive OR
$\wedge$	The symbol designating the logical operation of AND

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Table 6-2. Explanatory Notes

Note	Definition
Addressing Modes - Mode 0 Excluded	The applicability of the general addressing modes specified by the instruction's M field is stated. When mode zero is encountered and is excluded a specification violation occurs.
Special Addresses	The allowed set of hardware registers is stated for effective operand addresses in the range of 0000_{16} to $003F_{16}$. Access to addresses 20_{16} to $3F_{16}$ is only permitted when specified in the instruction. Modification of the contents of addresses 20_{16} to $3F_{16}$ requires privileged program level status. See also table 6-9.
Mode 0 with Indexing	The occurrence and consequence of carry out of the sign position or overflow during literal indexing addressing mode is stated. The index register is treated as a 32 bit quantity.
Deficient Result	Refers to the 32 bit result that occurs when the overflow indicator is set on an algebraic operation. The 31 value bits of the result are correct; the sign bit of this result is the complement of the correct result.
Excess half word	Refers to a number which exceeds the range of a 16-bit half word. A 32-bit word represents a half word number in its 16 least significant bit positions when the most significant 17 bits, bit positions 0 through 16 contain all ZEROS or all ONES.
Sign extended	Refers to a half word operand expanded to a word. The sign of half word, bit position 16, is extended into bit positions 0 through 15.
Not sign extended (or zero extended)	Refers to a half word operand expanded to a word; bit positions 0 through 15 are all ZEROS.

70061-14

the contents of the process register H. (Y) is not changed. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set only in mode 0 with indexing. The excess indicator is set only in mode 0 with indexing. Trap on overflow occurs only in mode 0 with indexing and only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
20	LDF	Y,H	(Y) → H	4.5

70061-402

(1) All address modes are permitted.

(2) Special addresses: all, see tables 6-2 and 6-9 (privilege not required).

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. If indexing exceeds a word, then overflow indicator is set and deficient result is loaded into H.

Example	Addressing Mode	Action
LDF YBLT,12	Direct	The 32 bit content of address YBLT is loaded into Process Register 12.

70061-403

b. *Load Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) with extended sign replaces the contents of the process register H. (Y) is not changed. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set only in mode 0 with indexing. The excess indicator is set only in mode 0 with indexing. Trap on overflow occurs only in mode 0 with indexing and only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
60	LDH	Y,H	$(Y)_s$ → H	4.5

70061-404

(1) All address modes are permitted.

(2) Special addresses: all, see tables 6-2 and 6-9 (privilege not required).

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. If indexing exceeds a word, then overflow indicator is set and deficient result is loaded into H.

Example	Addressing Mode	Action
LDH =155,9	Literal	The sign extended decimal literal is loaded into Process Register 9.

70061-405

c. *Load Most Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) replaces the contents of bit positions 0 thru 15 of the process register H. Bit positions 16 thru 31 of (H) are not changed. (Y) is not changed. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set only in mode 0 with indexing. The excess indicator is set only in mode 0 with indexing. Trap on overflow occurs only in mode 0 with indexing and only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
24	LMH	Y,H	$(Y) \rightarrow H_{0\ 15}$	4.5

70061-406

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. If indexing exceeds a word, then overflow indicator is set and deficient result is loaded into H.

Example	Addressing Mode	Action
LMH $+10,14	Relative	The effective address is the ILR+10 (this instruction address +12). The 16 bit content of the effective address is loaded into bits 0 - 15 of Process Register 14. Bits 16 - 31 are not changed.

70061-407

d. *Load From Upper Byte.* Initially, the carry, overflow, and excess indicators are reset. The most significant eight bits (0 to 7 or 16 to 23) of the (Y) operand replace the contents of the least significant eight bits (24 to 31) of the process register H. Bits 0 to 23 of (H) are set to ZERO. (Y) is left unchanged. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set only in mode 0 with indexing. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only in mode 0 with indexing and only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
21	LDU	Y,H	$(Y)_U \rightarrow H_{24\ 31}$; $0 \rightarrow H_{0\ 23}$	4.5

70061-408

(1) All address modes are permitted.

(2) Special addresses: process registers only (half).

(3) Mode 0 with indexing: carry indicator is set by carry out of the word sign position. If indexing exceeds a word, then the overflow indicator is set and deficient result is loaded into H.

Example	Addressing Mode	Action
LDU CN+R'6',8	Direct with indexing	The contents of the most significant 8 bits (upper byte) of modified address CN are loaded into bits 24 - 31 of process register 8. Bits 0 - 23 of process register 8 are set to ZERO.

70061-409

e. *Load From Lower Byte.* Initially, the carry, overflow, and excess indicators are reset. The least significant eight bits (8 to 15 or 24 to 31) of the (Y) operand replace the contents of the least significant eight bits (24 to 31) of the process register H. Bits 0 to 23 of (H) are set to ZERO. (Y) is left unchanged. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set only in mode 0 with indexing. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only in mode 0 with indexing and only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
61	LDL	Y,H	$(Y)_L \rightarrow H_{24\text{-}31}$; $0 \rightarrow H_{0\text{-}23}$	4.5

70061-410

(1) All address modes are permitted.

(2) Special addresses: process registers only (half).

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. If indexing exceeds a word, then overflow indicator is set and deficient result is loaded into H.

Example	Addressing Mode	Action
LDL (TINT),5	Indirect	The contents of address TINT are a second address. The contents of the least significant 8 bits of the second address are loaded into bits 24 - 31 of process register 5. Bits 0 - 23 of process register 5 are set to ZERO.

70061-411

f. *Load Absolute Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) replaces the process register H if it is positive or zero. If (Y) is negative it is converted to the equivalent positive number (two's complement) and replaces (H). In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set when the operand (Y) is the maximum negative number, or in mode 0 with indexing; the result is stored in deficient form in H. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
22	LAF	Y,H	$\lvert(Y)\rvert \rightarrow H$	4.5

70061-412

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. The overflow indicator is set when the result exceeds a word.

Example	Addressing Mode	Action
LAF $+R'1'.15	Relative with indexing	The effective address is ILR + the contents of index register 1. The absolute value of the contents of the effective address is loaded into process register 15.

70061-413

g. *Load Absolute Half.* Initially the carry, overflow, and excess indicators are reset. The operand (Y) with extended sign replaces the process register H if it is positive or zero. If (Y) is negative it is sign extended and converted to the equivalent positive number (two's complement) and replaces (H). In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing if overflow occurs or the maximum negative number is generated. The overflow indicator is set only in mode 0 with indexing if overflow occurs or the maximum negative number is generated. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only in mode 0 with indexing and only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
62	LAH	Y,H	$\lvert(Y)_S\rvert \rightarrow H$	4.5

70061-414

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. Overflow indicator is set when result exceeds a word.

Example	Addressing Mode	Action
LAH =X'FA00',7	Literal	The absolute value of the sign extended hex literal is loaded into process register 7.

70061-415

h. *Load Two's Complement Full.* Initially, the carry, overflow, and excess indicators are reset. If the operand (Y) is a negative number, the positive equivalent is loaded into the process register (H). If the operand (Y) is a positive number, the negative equivalent is loaded into (H). The −(Y) represents the two's complement of (Y). A ZERO operand stays ZERO. In mode 0, The CA operand is sign extended. An operand exceeding a half word sets the excess indicator. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set when the operand (Y) is the maximum negative number, or in mode 0 with indexing; the result is stored in deficient form in H. Temporary overflow during indexing is accommodated. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
23	LCF	Y,H	$-(Y) \rightarrow H$	4.5

70061-416

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. Overflow indicator is set when result exceeds a word after complement operation.

Example	Addressing Mode	Action
LCF WWR+D'3',8	Direct with double indexing	The effective address is WWR as modified by the contents of index registers 1 and 3. The two's complement of the contents of the effective address is loaded into process register 8.

70061-417

i. *Load Two's Complement Half.* Initially, the carry, overflow, and excess indicators are reset. If the operand (Y) is a negative number, the positive equivalent with extended sign is loaded into the process register H. If the operand (Y) is a positive number, the negative equivalent with extended sign is loaded into (H). −(Y) represents the two's complement of (Y). A ZERO operand stays ZERO. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set only in mode 0 with indexing. Temporary overflow is accommodated. The excess indicator is set then the result exceeds a half word. Trap on overflow occurs only in mode 0 with indexing and only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
63	LCH	Y,H	$-(Y)_S \rightarrow H$	4.5

70061-418

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. Overflow indicator is set when result exceeds a word after a complement operation.

Example	Addressing Mode	Action
LCH =50+R'4',9	Literal with indexing	The two's complement of the sign extended modified decimal literal is loaded into process register 9.

70061-419

6-6. Store (Register) Instructions

The following paragraphs describe the store (register) instructions.

a. *Store Full.* Initially, the carry, overflow, and excess indicators are reset. The process register (H) is stored in address Y (H) is not changed. If the program activity register is addressed, a program level change is not attempted. The carry indicator is never set. The overflow indicator is never set. The excess indicator is set when (H) exceeds a half word. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
26	SDF	Y,H	$(H) \rightarrow Y$	4.8

70061-420

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
SDF FIXD,11	Direct	The contents of process register 11 are stored into memory address FIXD.

70061-421

b. *Store Half.* Initially, the carry, overflow, and excess indicators are reset. The contents of bit positions 16 through 31 of process register (H) are stored in address Y. (H) is not changed. If the program activity register is addressed, a program level change is not attempted. If a page control and address register is addressed (20 to 2F hex) both the active register and its image in memory are modified. The carry indicator is never set. The overflow indicator is never set. The excess indicator is set when (H) exceeds a half word.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
66	SDH	Y.H	$(H)_{16\ 31} \rightarrow Y$	4.8

70061-422

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
SDH R'8',10	Direct	The contents of bits 16 - 31 of process register 10 are stored in bits 0 - 15 of process register 8.

70061-423

c. *Store Most Half.* Initially, the carry, overflow, and excess indicators are reset. The contents of bit positions 0 thru 15 of the process register H are stored into address Y. (H) is not changed. If the program activity register is addressed, a program level change is not attempted. If a page control and address register is addressed (20 to 2F hex) both the active register and its image in memory are modified. The carry indicator is never set. The overflow indicator is never set. The excess indicator is set when (H) exceeds a half word.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
64	SMH	Y.H	$(H)_{0\ 15} \rightarrow Y$	4.8

70061-424

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
SMH (TD+R'7'),2	Indirect with indexing	The contents of modified address TD are a second address. The contents of bits 0 - 15 of process register 2 are stored in the second address.

70061-618

d. *Store Into Upper Byte.* Indicators are not affected. The least significant eight bits (24 to 31) of the process register (H) are stored in bit positions (0 to 7 or 16 to 23) of address Y. Bit positions (8 to 15 or 25 to 31) in address Y are left unchanged. (H) is left unchanged.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
25	SDU	Y.H	$(H)_{24\ 31} \rightarrow Y_U$. Y_L unchanged	5.0

70061-425

(1) Address mode 0 is extended.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
SDU BNT-\$,13	Relative	The effective address is address BNT minus the ILR. The contents of bits 24 - 31 of process register 13 are stored in the most significant 8 bit positions of the effective address. The least significant 8 bits are unchanged.

70061-426

e. *Store Into Lower Byte.* Indicators are not affected. The least significant eight bits (24 to 31) of the process register H are stored in bit positions (8 to 15 or 24 to 31) of address Y. Bit positions (0 to 7 or 16 to 23) in address Y are left unchanged. (H) is left unchanged.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
65	SDL	Y.H	$(H)_{24\ 31} \rightarrow Y_L$. Y_U unchanged	5.0

70061-427

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
SDL (FLT6),10	Indirect	The contents are address FLT6 are a second address. The contents of bits 24 - 31 of process register 10 are stored in the least significant 8 bits of the second address. The most significant 8 bits are unchanged.

70061-428

6-7. Move Instructions

Move instructions are described in the following paragraphs.

a. *Move All ZEROS Full.* Indicators are not affected. The content of address Y is reset to all ZEROS (32 bits). If the program activity register is addressed, a program level change is not attempted. The H field is not used.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
27	MZF	Y	0 → Y	4.8

70061-429

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

(3) Memory word parity is not detected prior to the storage of the ZERO word.

Example	Addressing Mode	Action
MZF SINCO	Direct	The 32 bit content of address SINCO is reset to ZERO.

70061-430

b. *Move All ZEROS Half.* Indicators are not affected. The contents of the half word addressed by Y is reset to all ZEROS (16 bits). The adjacent half word is not changed. If the program activity register is addressed, a program level change is not attempted. The H field is not used.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
67	MZH	Y	0 → Y	4.8

70061-431

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

(3) Memory word parity is checked prior to the storage of the ZERO half word.

Example	Addressing Mode	Action
MZH $+16+R'1'	Relative with indexing	The effective address is the ILR + 16 + the contents of index register 1. The 16 bit content of the effective address is reset to ZERO.

70061-432

c. *Move Into Upper Byte.* Indicators are not affected. The contents of the immediate field (bit positions 8 thru 15 of the instruction word) are inserted in the upper byte of the half word, bit positions 0 to 7 or 16 to 23, of address Y. Bit positions 8 to 15 or 24 to 31 in address Y are left unchanged. I has a range of 0 to 255 decimal.

Figure 6-1 illustrates the immediate field for both the Move Into Upper Byte and Move Into Lower Byte instructions.

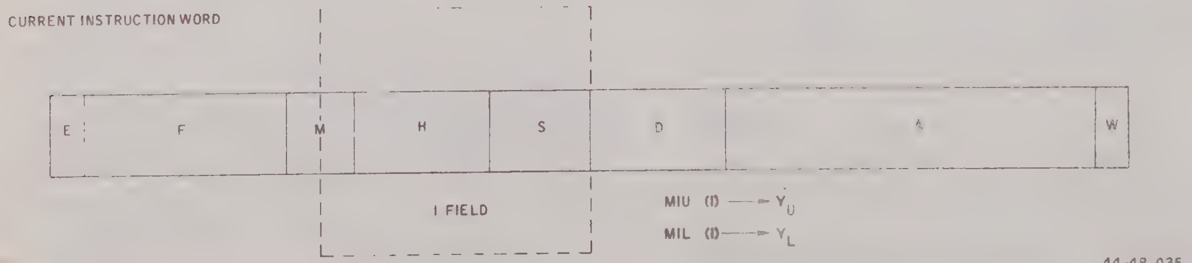


Figure 6-1. Move Into Upper Byte and Lower Byte Instructions

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
2D	MIU	Y, I	$(I) \rightarrow Y_U$, Y_L unchanged	5.0

70061-433

(1) No address mode modifications. Direct address (without indexing) mode is assumed.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
MIU FLGHT,74	Direct (The direct mode is always assumed with the MIU instruction.)	The contents of the immediate field of the current instruction word are placed in the most significant 8 bits of address FLGHT. The least significant 8 bits are unchanged (I field = 74 decimal).

70061-434

d. *Move Into Lower Byte.* Indicators are not affected. The contents of the immediate field (bit positions 8 thru 15 of the instruction word) are inserted in the lower byte of the half word, bit positions 8 to 15 or 24 to 31, of address Y. Bit positions 0 to 7 or 16 to 23 in address Y are left unchanged. I has a range of 0 to 255 decimal.

Figure 6-1 illustrates the immediate field for both the Move Into Upper Byte and Move Into Lower Byte instructions.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
6D	MIL	Y, I	$(I) \rightarrow Y_L$, Y_U unchanged	5.0

70061-435

(1) No address mode modifications. Direct address (without indexing) mode is assumed.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
MIL X'1000',200	Direct (The direct mode is always assumed with the MIL instruction.)	The contents of the immediate field of the current instruction word are placed in the least significant 8 bits of address hex 1000. The most significant 8 bits are unchanged. (I field = 200 decimal.)

70061-436

6-8. Exchange Instructions

Exchange Instructions are explained in the following paragraphs:

a. *Exchange Full.* Initially, the carry, overflow, and excess indicators are reset. The process register (H) is stored into address Y. The operand (Y) is loaded into the process register (H). The exchange is performed in a split memory cycle which is not interruptible. The carry indicator is never set. The overflow indicator is set when the initial value of the contents of (H) exceeds a half word.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
2E	EXF	Y, H	$(H) \rightarrow Y$, $(Y) \rightarrow H$	5.0

70061-437

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
EXF ARCTAN,11	Direct	The 32 bit content of address ARCTAN is placed in process register 11 and the 32 bit content of process register 11 is placed in address ARCTAN.

70061-438

b. *Exchange Half.* Initially, the carry, overflow, and excess indicators are reset. The contents of bit positions 16 thru 31 of process register (H) are stored into address Y. The operand (Y) with extended sign replaces the contents of the process register (H). The exchange is performed in a split memory cycle which is not interruptible. The carry indicator is never set. The overflow indicator is never set. The excess indicator is set when the initial $(H)_{16-31}$ exceeds a half word.

ic-tion Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
6E	EXH	Y, H	$(H)_{16\ 31} \rightarrow Y$, $(Y)_S \rightarrow H$	5.0

70061-439

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
EXH (FORET),4	Indirect	The contents of address FORET are a second address. The 16 bit content of the second address is sign extended and placed in process register 4. Bits 16 - 31 of process register 4 are placed in the second address.

70061-440

Section III. ARITHMETIC INSTRUCTIONS

6-9. General

Arithmetic instructions perform the addition, subtraction, multiplication and division functions of the computer in fixed point notation. There are seventeen instructions in this group.

6-10. Fixed Point Arithmetic Instructions

An extensive set of instructions is provided for accomplishing the full complement of binary arithmetic operations: add, subtract, multiply, and divide. Several variations of the basic binary addition and subtraction instructions are included for versatility in operand handling and selection. The two items in the operand field in each arithmetic instruction are the contents of the process register H and the contents of the memory location specified by the word address designator A as modified by the address mode designator M. Treatment of signs, placement of the result, and operand length selection are all discussed under the particular instruction. The correct positioning of operands is to be programmed prior to instruction execution. During all arithmetic operations the carry, overflow, and excess indicators are reset. The results of the operation, if one or more of these indicators are set, are explained under that particular instruction.

a. *Add Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is algebraically added to the process register (H). The sum replaces H. In mode 0, the CA operand is sign extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when result exceeds a word, and the deficient result is stored in H. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
08	ADF	Y, H	$(H) + (Y) \rightarrow H$	4.8

70061-441

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: overflow is accommodated.

Example	Addressing Mode	Action
ADF =600,9	Literal	Add the sign extended literal, 600 decimal, to the contents of process register 9 and store the result in process register 9.

70061-442

b. *Add Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) with extended sign is algebraically added to the process register (H), the sum replaces H. In mode 0, the CA operand is sign extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when the result exceeds a word, and the deficient result is stored in H. The excess indicator is set when result exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
48	ADH	Y, H	$(H) + (Y)_s \rightarrow H$	4.8

70061-443

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: overflow is accommodated.

Example	Addressing Mode	Action
ADH R'5',4	Direct	Takes the contents of the left most 16 bits of process register 5, sign extends the value for another 16 bits, adds the resulting value to the contents of process register 4 and stores the result in process register 4.

70061-444

c. *Add Logical Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically added as a 32 bit unsigned quantity to the process register (H). The sum replaces H. In mode 0, the CA operand is zero extended. The carry indicator is set by carry out word sign position. The overflow indicator is set when the result exceeds a word, and the deficient result is stored in H. The excess indicator is set when result exceeds a half word. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
0A	ALF	Y, H	$(H) + (Y) \rightarrow H$	4.8

70061-445

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator.

Example	Addressing Mode	Action
ALF =X'FA10',13	Literal	Adds the zero extended unsigned hex literal, FA10, to the signed contents of process register 13 and stores the signed result in process register 13.

70061-446

d. *Add Logical Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is not sign extended and is logically added as an unsigned 16 bit quantity to the 32 bit process register (H). The sum replaces H. In mode 0, the CA operand is zero extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when result exceeds a word, and the deficient result is stored in H. The excess indicator is set when result exceeds a half word. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
4A	ALH	Y, H	$(H) + (Y) \rightarrow H$	4.8

70061-447

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator.

Example	Addressing Mode	Action
ALH ABC,4	Direct	Takes the 16 bit unsigned zero extended contents of register ABC, adds it to the signed contents of process register 4 and stores the signed result in process register 4.

70061-448

e. *Replace Add Full.* Initially, the carry, overflow, and excess indicators are reset. The process register (H) is algebraically added to the operand (Y). The sum replaces Y. The process register (H) is not changed. The carry indicator is set by carry out of word sign position. The overflow indicator is set when the result exceeds a word, and the deficient result is stored in Y. The excess indicator is set when result exceeds a half word. Trap on overflow occurs only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
0E	RAF	Y, H	$(Y) + (H) \rightarrow Y$	5.2

70061-449

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RAF $+10,12	Relative	Adds the 32 bit content of the register specified by the ILR + 10 (this instruction address + 12) to the contents of process register 12 and stores the result in the specified operand address (ILR + 2 + 10).

70061-450

f. *Replace Add Half.* Initially, the carry, overflow, and excess indicators are reset. The process register (H) is algebraically added to the sign extended operand (Y). Bits 16 – 31 of the sum replaces Y. The process register (H) is not changed. The carry indicator is set by carry out of word sign position. The overflow indicator is set when result exceeds a word, the deficient result is stored in Y. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
4E	RAH	Y, H	$(Y)_s + (H) \to Y$	5.2

70061-451

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RAH TAB,6	Direct	Takes the 16 bit content of address TAB, sign extends the value another 16 bits, adds the result to the contents of process register 6 and stores the least significant 16 bits of the result in the operand address (TAB).

70061-452

g. *Subtract Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is algebraically subtracted from the process register (H). The difference replaces H. In mode 0, the CA operand is sign extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when result exceeds a word, and the deficient result is stored in H. The excess indicator is set when the result exceeds half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
09	SBF	Y, H	$(H) - (Y) \to H$	4.8

70061-453

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: overflow is accommodated.

Example	Addressing Mode	Action
SBF (ALLOT),11	Indirect	The contents of address ALLOT are taken as a 16 bit second address. The contents of the second address are subtracted from the contents of process register 11 and the result is stored in process register 11.

70061-454

h. *Subtract Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) with extended sign is algebraically subtracted from the process register (H). The difference replaces H. In mode 0, the CA operand is sign extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when result exceeds a word, and the deficient result is stored in H. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
49	SBH	Y, H	$(H) - (Y)_s \to H$	4.8

70061-455

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: overflow is accommodated.

Example	Addressing Mode	Action
SBH =0+R'2',8	Literal with indexing	The literal in this example is the contents of index register 2. The literal is sign extended 16 bits, subtracted from the contents of process register 8 and the result is stored in process register 8.

70061-456

i. *Subtract Logical Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically subtracted as a 32 bit unsigned quantity from the process register (H). The difference replaces H. In mode 0, the CA operand is zero extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when the result exceeds a word, and the deficient result is stored in H. The excess indicator is set when the result exceeds a half word. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
0B	SLF	Y, H	(H) - (Y) → H	4.8

70061-457

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator.

Example	Addressing Mode	Action
SLF BLD+R'2',5	Direct with indexing	The effective address is BLD as modified by the contents of index register 2. The unsigned 32 bit content of the effective address is subtracted from the signed contents of process register 5, the signed result is stored in process register 5.

70061-458

j. *Subtract Logical Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is not sign extended and is logically subtracted as an unsigned 16 bit quantity from the 32 bit process register (H). The difference replaces H. In mode 0, the CA operand is zero extended. The carry indicator is set by carry out of word sign position. The overflow indicator is set when the result exceeds a word, and the deficient result is stored in H. The excess indicator is se when the result exceeds a half word. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
4B	SLH	Y, H	(H) - (Y) → H	4.8

70061-459

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator.

Example	Addressing Mode	Action
SLH $-20,14	Relative	Effective address = ILR-20. The unsigned 16 bit content of the effective address is subtracted from the signed contents of process register 14 and the signed result is stored in process register 14.

70061-460

k. *Replace Subtract Full.* Initially, the carry, overflow, and excess indicators are reset. The process register (H) is algebraically subtracted from the operand (Y). The difference replaces Y. The process register (H) is not changed. The carry indicator is set by carry out of word sign position. The overflow indicator is set when the result exceeds a word, and the deficient result is stored in Y. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
0F	RSF	Y, H	(Y) - (H) → Y	5.2

70061-461

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RSF ABLE,15	Direct	Subtracts the contents of process register 15 from the contents of address ABLE and stores the result in address ABLE.

70061-462

Replace Subtract Half. Initially, the carry, overflow, and excess indicators are reset. The process register (H) is algebraically subtracted from the sign extended operand (Y). Bits 16 – 31 of the difference replace Y. The process register (H) is not changed. The carry indicator is set by carry out of word sign position. The overflow indicator is set when result exceeds a word, and the deficient result is stored in Y. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
4F	RSH	Y, H	$(Y)_s - (H) \rightarrow Y$	6.2

70061-463

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RSH (ZETA),1	Indirect	The 16 bit content of address ZETA is a second address. The contents of process register 1 are subtracted from the sign extended 16 bit content of the second address and the least significant 16 bits of the result are stored in the second address.

70061-464

m. *Multiply Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is multiplied by the process register (H). H may specify either an even or odd process register. The double word product replaces the process register pair H_e, H_o; (H_o) will contain the least significant bits of the product. Figure 6-2 illustrates the results of the instruction execution. In mode 0, the CA operand is sign extended. The carry indicator is set when the result exceeds a word. Overflow can only occur in mode 0 with indexing. The excess indicator is set when the result exceeds a half word. Trap can only occur in mode 0 with indexing.

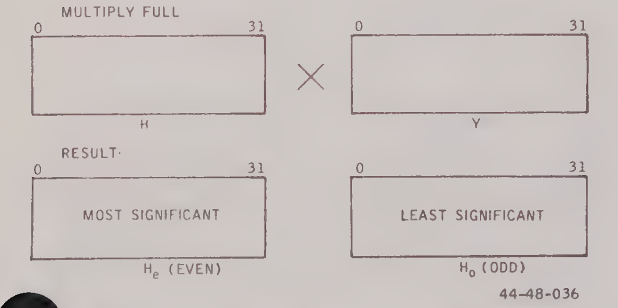


Figure 6-2. Multiply Full Instruction Execution

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
0C	MPF	Y, H	$(H) \times (Y) \rightarrow H_e, H_o$	16.4

70061-465

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: if indexing exceeds a word, then overflow indicator is set, instruction terminates with (H) and (Y) unchanged and carry and excess indicators reset. Trap occurs when OT indicator is zero.

NOTE

The carry indicator is not set when the most significant 32 bits and bit 0 of the least significant 32 bits of the double word product are either all ZEROS or all ONES. Thus (H_o) contains a word product.

Example	Addressing Mode	Action
MPF =O'456',10	Literal	The contents of process register 10 are multiplied by the sign extended octal literal. The least significant 32 bits of the result are placed in process register 11 and the most significant 32 bits of the result are placed in process register 10.

70061-466

n. *Multiply Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) with extended sign is multiplied by process register (H). The word product replaces H. Figure 6-3 illustrates the results of the instruction execution. In mode 0, the CA operand is sign extended. The carry indicator is set when the result exceeds a word, and the least significant 32 bits of the product are stored in H; the most significant bits are lost. The excess indicator is set when the result exceeds a half word. Trap can only occur in mode 0 with indexing.

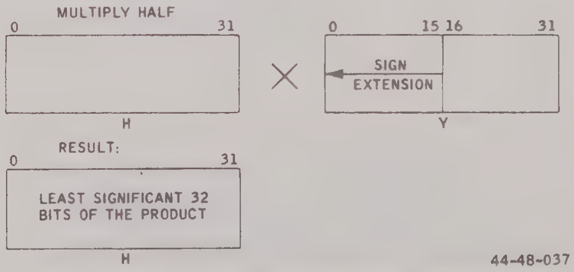


Figure 6-3. Multiply Half Instruction Execution

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
4C	MPH	Y, H	$(H) \times (Y)_s \rightarrow H$	16.4

70061-467

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: if indexing exceeds a word, then overflow indicator is set, instruction terminates with (H) and (Y) unchanged and carry and excess indicators reset. Trap occurs when OT indicator is zero.

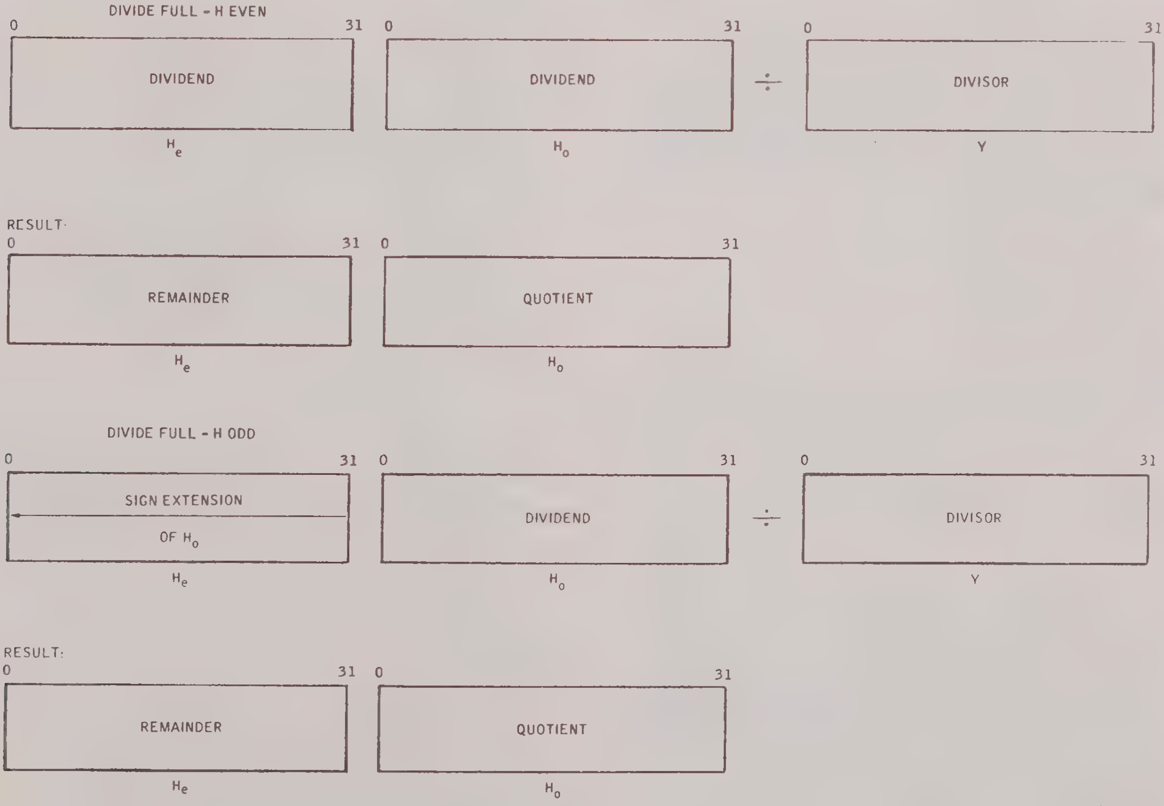
NOTE

The carry indicator should be tested to assure that the result did not exceed a word.

Example	Addressing Mode	Action
MPH $+R'1',7	Relative with indexing	Effective address = ILR + contents of index register 1. The 16 bit content of the effective address is sign extended, multiplied by the contents of process register 7 and the least significant 32 bits of the product are stored in process register 7.

70061-468

o. *Divide Full.* Initially, the carry, overflow, and excess indicators are reset. If H is even, then the process register pair (H_e,H_o) is divided by the operand (Y). If H is odd, then the process register (H_o) with extended sign is divided by the operand (Y). The quotient replaces H_o. The remainder replaces H_e. The sign of a non-zero remainder equals the sign of the dividend (H); a zero remainder is positive. The division is an "integer" division (see chapter 5). Figure 6-4 illustrates


DIVIDE FULL - H EVEN
0
31
DIVIDEND
He
0
31
DIVIDEND
Ho
÷
0
31
DIVISOR
Y
RESULT
0
31
REMAINDER
He
0
31
QUOTIENT
Ho
DIVIDE FULL - H ODD
0
31
SIGN EXTENSION
OF Ho
He
0
31
DIVIDEND
Ho
÷
0
31
DIVISOR
Y
RESULT:
0
31
REMAINDER
He
0
31
QUOTIENT
Ho

44-48-038

Figure 6-4. Divide Full — H Even and H Odd Instructions Execution

results of the instruction execution. In mode 0, the A operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set when the quotient exceed a word, the divisor (Y) is zero or overflow occurs during literal indexing; no division takes place, and H_e and H_o are left unchanged and the excess indicator is reset. The excess indicator is set when the quotient exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (µsec)
OD	DIF	Y, H	(H_e, H_o) or $(H_o)_s$ ÷ (Y) → H_o Remainder → H_e	18.1

70061-469

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry indicator is set by carry out of word sign position. If indexing exceeds a word then overflow indicator is set, instruction terminates with (H) and (Y) unchanged, and trap occurs when OT indicator is zero.

Example	Addressing Mode	Action
DIF CUTL,2	Direct	The contents of process registers 2 and 3 are divided by the 32 bit content of address CUTL. The quotient is placed in process register 3 and the remainder is placed in process register 2.

70061-470

When absolute value of divisor is larger than the absolute value of dividend then the quotient will be zero (7 ÷ 8 = 0, remainder = 7).

For H odd overflow occurs for the following two conditions: Divisor is zero, or dividend is 8000 0000 and divisor is FFFF FFFF (largest negative number ÷ smallest negative number).

For H even overflow occurs when divisor is zero or quotient Q exceeds one word, i.e.,

$$Q > +2^{31} - 1 = 7\,FFF\;\;FFFF_{16} \text{ or}$$
$$Q < -2^{31} = 8\,000\;\;0000_{16}$$

70061-800

H odd examples (decimal/hexadecimal)

Dividend:	+7	=	0000 0007
Divisor:	+2	=	0000 0002
Quotient:	+3	=	0000 0003
Remainder:	+1	=	0000 0001
Dividend:	-7	=	FFFF FFF9
Divisor:	+2	=	0000 0002
Quotient:	-3	=	FFFF FFFD
Remainder:	-1	=	FFFF FFFF
Dividend:	-7	=	FFFF FFF9
Divisor:	-2	=	FFFF FFFE
Quotient:	+3	=	0000 0003
Remainder:	-1	=	FFFF FFFF
Dividend:	+7	=	0000 0007
Divisor:	-2	=	FFFF FFFE
Quotient:	-3	=	FFFF FFFD
Remainder:	+1	=	0000 0001
Dividend:			4000 0006
Divisor:			4000 0000
Quotient:			0000 0001
Remainder:			0000 0006

H even examples

Dividend:	0000 0002	0000 0003
Divisor:		4000 0000
Quotient:		0000 0008
Remainder:		0000 0003
Dividend:	0200 0000	0000 0003
Divisor:		4000 0000
Quotient:		0800 0000
Remainder:		0000 0003

70061-1005

p. *Divide Half.* Initially, the carry, overflow, and excess indicators are reset. The process register (H) is divided by the operand (Y) with extended sign. The quotient replaces (H_o); the remainder replaces (H_e); the sign of a non-zero remainder equals the sign of the

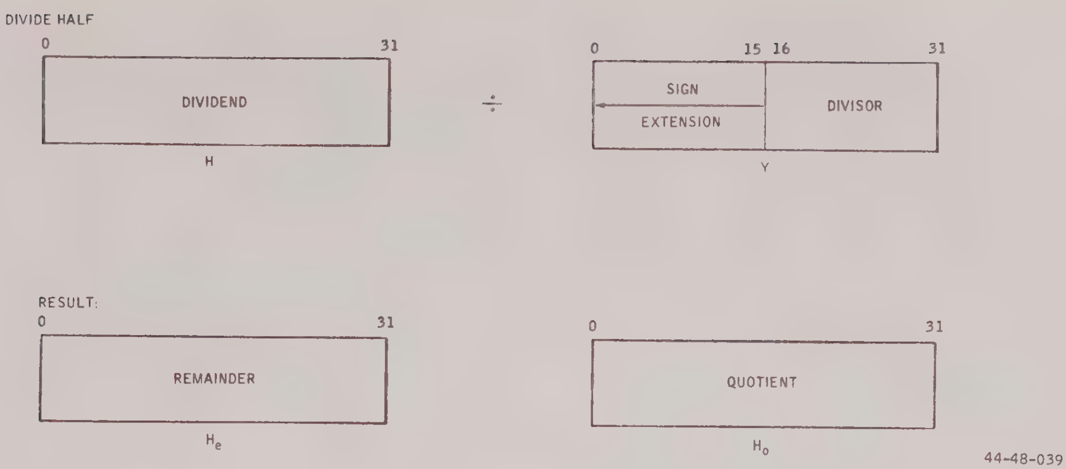


Figure 6-5. Divide Half Instruction Execution

dividend (H); a zero remainder is positive. Figure 6-5 illustrates the result of instruction execution. In mode 0, the CA operand is sign extended. The carry indicator is set only in mode 0 with indexing. The overflow indicator is set when the quotient exceeds a word or the divisor is zero or overflow occurs during literal indexing; no division takes place, and (H) and (Y) are left unchanged and the excess indicator is reset. The excess indicator is set when the quotient exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
4D	DIH	Y,H	$(H) \div (Y)_S \rightarrow H_o$ Remainder $\rightarrow H_e$	18.1

70061-471

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing; carry indicator is set by carry out of word sign position. If indexing exceeds a word then overflow indicator is set, instruction terminates with (H) and (Y) unchanged, and trap occurs when OT indicator is zero.

Example	Addressing Mode	Action
DIH =100,3	Literal	The contents of process register 3 are divided by the sign extended decimal literal. The quotient is placed in process register 3 and the remainder is placed in process register 2.

70061-472

When absolute value of divisor is larger than the absolute value of dividend then the quotient will be zero ($7 \div 8 = 0$, remainder $= 7$).

Overflow occurs for the following two conditions: Divisor is zero, or dividend is $8000\ 0000_{16}$ and divisor is $FFFF_{16}$ (largest negative number ÷ smallest negative number).

For other examples see divide full instruction.

q. *Replace Square Root Full.* Initially, the carry, overflow, and excess indicators are reset. The argument (H) is treated as an integer of sign plus 31 bits of value followed by 32 assumed ZERO fraction bits. The square root of process register (H) replaces the 32 bits of Y. The carry indicator is never set. The overflow indicator is set when (H) is negative; instruction is not executed, and (H) and (Y) are left unchanged and the excess indicator is reset. The excess indicator is set when the result exceeds a half word. Trap on overflow occurs only when the OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
1B	RQF	Y, H	$\sqrt{(H)} \rightarrow Y$	16.6

70061-473

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

NOTE

If (H) is not an exact square, the 32 bits of Y are replaced by the largest integer less than the square root of (H).

Example	Addressing Mode	Action
RQF CC+R'7',12	Direct with indexing	The square root of the contents of process register 12 is obtained and it is stored in the operand address CC as modified by index register 7.

70061-474

Section IV. TRANSFER INSTRUCTIONS

6-11. Introduction

Transfer instructions provide for program transfers depending on certain criteria specified by each instruction. The transfers are accomplished by substituting the contents of the operand Z* for the next instruction in sequence (see table 5-2).

6-12. Transfers and the Rules of Addressing

To avoid programming complications, the rules of addressing for the AN/GYK-12 Computer must be followed for all transfer instructions. If the direct mode (mode 1) of addressing is specified, it is the contents of the operand address that becomes the transfer address. If the literal mode (mode 0) is specified then the literal address becomes the transfer address, and so on. A list of examples, following the first transfer instruction description, illustrates the effect of a transfer in each of the various addressing modes. These rules must be followed for all the transfer instructions, whether they be unconditional or conditional transfers.

6-13. Use of Transfer Instructions

Transfer instructions have many uses. There are transfers which are unconditional where a transfer must take place and there are transfers which are conditional where a transfer only takes place if a certain specified condition is met. The unconditional transfers are used to transfer control from one part of a program to another or to enter subroutines. The conditional transfers are used to test bits in special registers, to test switches on the computer test set (CTS), to test and increment or decrement the contents of index registers and to test the contents of process registers.

6-14. Control Transfer Instructions

The following paragraphs describe the control transfer instructions:

a. *Transfer Unconditionally.* Indicators are not affected. The transfer address Z* becomes the address of the next instruction by replacing the contents of the instruction location register. H is not used.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
30	XFR	Y	$Z^* \rightarrow ILR$	4.5

70061-475

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XFR = CHAR	Literal	Transfer to address CHAR.
XFR CHAR	Direct	Transfer to the address specified by the contents of CHAR.
XFR $+24	Relative	Transfer to the address specified by the ILR+24 (this instruction address +26).
XFR (CHAR)	Indirect	The contents of address CHAR are a second address. Transfer to the address specified by the contents of the second address.

70061-476

b. *Transfer and Store Link.* Indicators are not affected. The content of the instruction location register is the address of the next instruction in sequence. This address is stored in bit positions 16 thru 31 of process register (H); bit positions 0 thru 15 of (H) are left unchanged. The transfer address Z* becomes the address of the next instruction by replacing the contents of the instruction location register.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
70	XLK	Y, H	(ILR) → H; Z* → ILR	4.5

70061-477

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XLK =TEMP,15	Literal	Stores the contents of the ILR (which is the address of the next instruction in sequence) in bits 16 - 31 of process register 15 and transfers to address TEMP. Bits 0 - 15 of process register 15 are unchanged.

70061-478

c. *Transfer on Indicators.* Indicators are not affected. A bit-for-bit comparison is made between the instruction's H field and the conditions of four indicator flip-flops: carry, overflow/greater, equal/excess, and less. If any ONE bit of the H field corresponds to the ON state of the indicator, a transfer to address Z* takes place. Otherwise, the next instruction in normal sequence is obtained. Also, the next instruction is obtained when H = 0. Figure 6-6 illustrates the various values of the H field and the indicator(s) each value tests.

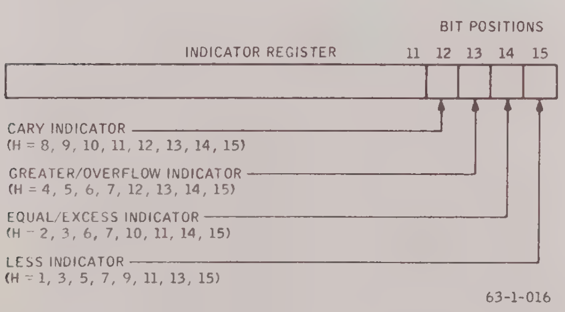

BIT POSITIONS
INDICATOR REGISTER
11
12
13
14
15
CARY INDICATOR
(H = 8, 9, 10, 11, 12, 13, 14, 15)
GREATER/OVERFLOW INDICATOR
(H = 4, 5, 6, 7, 12, 13, 14, 15)
EQUAL/EXCESS INDICATOR
(H = 2, 3, 6, 7, 10, 11, 14, 15)
LESS INDICATOR
(H = 1, 3, 5, 7, 9, 11, 13, 15)
63-1-016

Figure 6-6. Indicator Register

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
71	XIN	Y, H	If Ind$_i$ = H$_i$, Z* → ILR Otherwise, no operation H = 0, no operation	4.5

70061-479

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XIN EQ,2	Direct	If the EQUAL/EXCESS indicator in the indicator register is set to 1 a transfer takes place to the address specified by the contents of EQ. If the indicator is not set to 1 the next instruction in sequence is executed.

70061-480

NOTE

The assembler for the AN/GYK-12 Computer makes available to the coder eight extended mnemonics for the XIN instruction. The list of the extended mnemonics and the action of each appears in the table below. A coding example follows the table. These instructions are discussed in detail in the AN/GYK-12 Computer Assembly Language Manual.

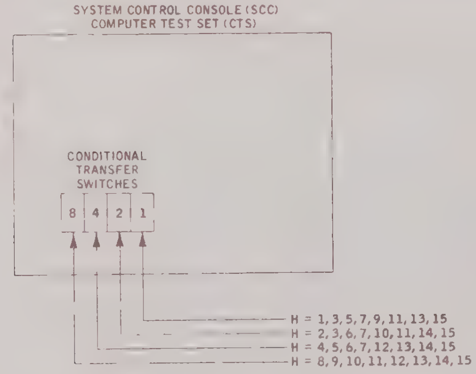
Extended Mnemonic*	Action	Implied Value of H
XLS	Transfer on Less	1
XGR	Transfer on Greater	4
XEQ	Transfer on Equal	2
XNG	Transfer on Not Greater	3
XNL	Transfer on Not Less	6
XNE	Transfer on Not Equal	5
XCY	Transfer on Carry	8
XOF	Transfer on Overflow	4

*See the AN/GYK-12 Computer Assembly Language Manual

Example	Addressing Mode	Action
XCY = NOT	Literal	If the CARRY indicator is set to 1 a transfer to address NOT takes place. If the indicator is not set to 1 the next instruction in sequence is executed. This instruction is the equivalent of: XIN = NOT,8

70061-481

d. *Transfer on Test Switches.* Indicators are not affected. A bit-for-bit comparison between the on and off states of four conditional transfer switches, TSW, of the Computer Test Set (CTS) or System Control Console (SCC) and the H field is made. If any switch is ON and its corresponding bit in the H field is a ONE, a transfer to address Z* occurs. Otherwise the next instruction in normal sequence is obtained. Also, the next instruction in sequence is obtained when H = 0, or if there is no CTS and SCC present. Figure 6-7, illustrates the various values of the H field and the switch(es) each value tests.


SYSTEM CONTROL CONSOLE (SCC)
COMPUTER TEST SET (CTS)
CONDITIONAL TRANSFER SWITCHES
8
4
2
1
H = 1, 3, 5, 7, 9, 11, 13, 15
H = 2, 3, 6, 7, 10, 11, 14, 15
H = 4, 5, 6, 7, 12, 13, 14, 15
H = 8, 9, 10, 11, 12, 13, 14, 15

70061-181

Figure 6-7. CTS/SCC Conditional Transfer Switches

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
31	XSW	Y,H	If $TSW_i = H_i$, $Z^* \rightarrow ILR$ Otherwise, no operation If H = 0, no operation If H ≠ 0 and no Test Set, no operation	4.5

70061-483

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XSW $+10,4	Relative	The effective transfer address is the ILR+10. If conditional transfer switch 4 is in the on position, a transfer to the effective address takes place. If the switch is not in the on position, the next instruction in sequence is executed.

70061-484

e. *Execute.* Indicators are not affected. The transfer address Z* is used as the address of the next instruction. This 32-bit word (Z*) is placed into the computer's instruction register. After this instruction is executed, the next instruction in normal sequence is obtained. If the instruction to be executed calls for a transfer, then the transfer takes place. H is not used.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
36	XEX	Y	$Z^* \rightarrow ILR$, INTERIM	4.5

70061-485

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XEX =OPER+R'4'	Literal with indexing	The one instruction located at the modified address OPER is executed out of sequence. Control then returns to the instruction following the XEX. If the instruction to be executed out of sequence is a transfer instruction, the transfer is executed and control will not be returned to the instruction following the XEX.

70061-486

6-15. Index Test Instructions

The following paragraphs describe the index test instructions:

a. *Test, Conditionally Decrement by One and Transfer.* Indicators are not affected. Bits 16 to 31 of process register (H) are treated as an unsigned 16 bit number (index quantity). If this number is not ZERO, it is reduced by one and transfer to address Z* takes place. If the number is ZERO, it is not changed and the next instruction in normal sequence is obtained. Bits 0 to 15 of (H) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
34	XDO	Y,H	If $(H) \neq 0$; $(H)-1 \rightarrow H$, $Z^* \rightarrow ILR$ If $(H) = 0$; no operation	4.8

70061-487

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XDO FILT,7	Direct	The content of index register 7 is tested. If it is ZERO, the next instruction in sequence is executed. If not ZERO, the content is decremented by 1 and a transfer to the address specified by the contents of FILT takes place.

70061-488

b. *Test, Conditionally Decrement by Two and Transfer.* Indicators are not affected. Bits 16 to 31 of process register (H) are treated as an unsigned 16 bit number (index quantity). If this number is not ZERO and not ONE, it is reduced by two and transfer to address Z* takes place. If the number is ZERO, or ONE, it is not changed and the next instruction in normal sequence is obtained. Bits 0 to 15 of (H) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
74	XDT	Y, H	If $(H) \neq 0$ or 1; $(H)-2 \rightarrow H$, $Z^* \rightarrow ILR$ If $(H) = 0$ or 1; no operation	4.8

70061-489

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XDT =AGAIN,6	Literal	The content of index register 6 is tested. If it is ZERO or ONE, the next instruction in sequence is executed. If not ZERO or ONE, the content is decremented by 2 and a transfer to address AGAIN takes place.

70061-490

c. *Test, Conditionally Increment by One and Transfer.* Indicators are not affected. Bits 16 to 31 of process register (H) are treated as an unsigned 16 bit number (index quantity). If this number is not ZERO, it is increased by one and transfer to Z* takes place. If the number is ZERO, it is not changed and the next instruction in normal sequence is obtained. Bits 0 to 15 of (H) are not changed. Incrementing the largest magnitude number by one results in ZERO being put in bits 16 to 31 of (H).

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
35	XIO	Y, H	If $(H) \neq 0$; $(H)+1 \rightarrow H$, $Z^* \rightarrow ILR$ If $(H) = 0$; no operation	4.8

70061-491

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XIO =X'FAO'.5	Literal	The content of index register 5 is tested. If it is ZERO, the next instruction in sequence is executed. If it is not ZERO, the content is incremented by 1 and a transfer to hex address FA0 takes place.

70061-492

d. *Test, Conditionally Increment by Two and Transfer.* Indicators are not affected. Bits 16 to 31 of process register (H) are treated as an unsigned 16 bit number (index quantity). If this number is not ZERO and not ONE, it is increased by two and transfer to address Z* takes place. If the number is ZERO or ONE, it is not changed and the next instruction in normal sequence is obtained. Bits 0 to 15 of (H) are not changed. Incrementing the largest magnitude by two results in ONE being put in bits 16 to 31 of (H). Incrementing the second largest magnitude number by two results in ZERO being put in bits 16 to 31 of (H).

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)

75	XIT	Y, H	If (H) $\neq$ 0 or 1;
			(H)+2 → H,
			Z* → ILR
			If (H) = 0 or 1;
			no operation
				4.8

70061-493

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XIT BB+R'2',4	Direct with indexing	The content of index register 4 is tested. If it is ZERO or ONE, the next instruction in sequence is executed. If not ZERO or ONE, the content is incremented by 2 and a transfer specified by the contents of modified address BB takes place.

70061-494

6-16. Process Register Test Instructions

a. *Transfer if Process Register is Zero.* Indicators are not affected. If the process register H is ZERO, a transfer to address Z* occurs; otherwise, the next instruction in normal sequence is obtained. (H) and (Y) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)

32	XEF	Y, H	If (H) = 0;
			Z* → ILR
			If (H) $\neq$ 0;
			no operation
				4.5

70061-495

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XEF $+R'1',11	Relative with indexing	The effective transfer address is the ILR + the content of index register 1. If the contents of process register 11 are ZERO a transfer to the effective address takes place. If not ZERO, the next instruction in sequence is executed.

70061-496

b. *Transfer if Process Register is not ZERO.* Indicators are not affected. If the process register (H) is not ZERO, a transfer to address Z* occurs. Otherwise, the next instruction in normal sequence is obtained. (H) and (Y) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)

72	XUF	Y,H	If (H) $\neq$ 0;
			Z* → ILR
			If (H) = 0;
			no operation
				4.5

70061-497

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XUF =TY+R'3',1	Literal with indexing	If the contents of process registers 1 are not ZERO, a transfer to the modified address TY takes place. If the contents are ZERO, the next instruction in sequence is executed.

70061-498

c. *Transfer if Process Register is Positive.* Indicators are not affected. If the sign bit of process register (H) is a ZERO (positive or zero number), a transfer to address Z* occurs. Otherwise, the next instruction in normal sequence is obtained. (H) and (Y) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)

33	XPF	Y, H	If (H) ≥ 0;
			Z* → ILR
			If (H) < 0;
			no operation
				4.5

70061-499

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XPF XFER,14	Direct	If the contents of process register 14 are positive, a transfer to the address specified by the contents of XFER takes place. If the contents are not positive, the next instruction in sequence is executed.

70061-500

d. *Transfer if Process Register is Negative.* Indicators are not affected. If the sign bit of the process register (H) is a ONE (negative), a transfer to address Z* occurs. Otherwise, the next instruction in normal sequence is obtained. (H) and (Y) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)

73	XNF	Y, H	If (H) < 0;
			Z* → ILR
			If (H) ≥ 0;
			no operation
				4.5

70061-501

(1) All (transfer) address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
XNF =BEGIN,9	Literal	If the contents of process register 9 are negative, a transfer to address BEGIN takes place. If the contents are not negative, the next instruction in sequence is executed.

70061-502

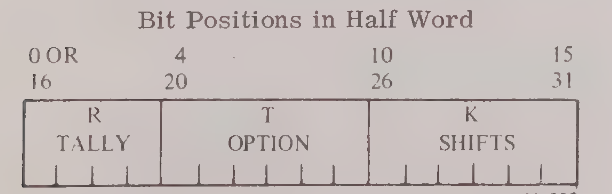
Section V. SHIFT INSTRUCTIONS

6-17. Introduction

There are two operation codes that specify a shift operation for the AN/GYK-12 Computer. One function code specifies a full word or double word shift and the other function code specifies a half word shift. In all cases it is the contents of process registers which are shifted.

6-18. The Operand of Shift Instructions

All shift instructions require a 16-bit operand which has three fields. An illustration of the operand is shown in the chart below.



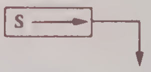
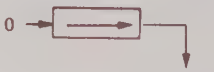
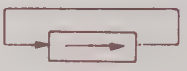
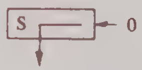
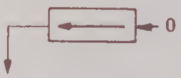
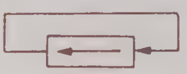
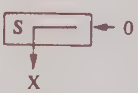
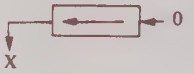
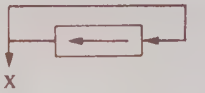
70061-503

a. *R.* This field is four bits in length and occupies the first four bits of the half word operand. It will contain a number from 0 – 15 which will stand for a process register. This field is not used in all shifting options and those options which do not use the R field will ignore these four bits. The normal function of this register is to hold a count or tally, for certain shift options.

b. *T.* This field is six bits in length and immediately follows the R field. The T field will contain a number which specifies one of the many shift options which are available. There are nine options available for full word shifts, eight options available for double word shifts and nine options available for half word shifts. The value of T for each shift option and the function of each option performs is illustrated in tables 6-3, 6-4, and 6-5. Operations for values of T not listed is undefined.

c. *K.* This field is six bits in length and immediately follows the T field. The K field specifies the number of bit positions to be shifted. A number from 0 – 63 may be placed in this field. A K field equal to ZERO specifies no shift.

Table 6-3. Shift Full Word Instructions

Hex T	Shift Type	Extended Mnemonic*	Process Register	Comment
00	Algebraic, Right, (Linear), Full Word	SARF		Sign Extended (S = Sign Bit)
04	Logical, Right, (Linear), Full Word	SLRF		
05	Circular, Right, Full Word	SCRF		
02	Algebraic, Left, (Linear), Full Word	SALF		S is not modified
06	Logical, Left, (Linear), Full Word	SLLF		
07	Circular, Left, Full Word	SCLF		
12	Normalize, Full Word	SNF		Shift until X ≠ S or K = 0 K - Shifts → R
[illegible]6	Shift and Count, (Linear), Full Word	SCF		Shift until K = 0 Count X = 1's (R (Tally)) + Count → R
17	Shift and Count, Circular, Full Word	SCCF		Shift until K = 0 Count X = 1's (R (Tally)) + Count → R

*See the AN/GYK-12 Computer Assembly Language Reference Manual, USACSCS-TF-4-2

70061-15

6-19. Extended Mnemonics For Shift Instructions

The AN/GYK-12 Assembler provides extended mnemonics for each shift option available for full, double and half word shifts. Tables 6-3, 6-4 and 6-5 illustrate the extended mnemonic for each option. A detailed discussion of the extended mnemonics for shift instructions is provided in the AN/GYK-12 Computer Assembly Language Reference Manual, USACSCS-TF-4-2.

6-20. Instructions

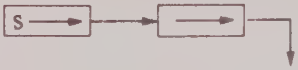
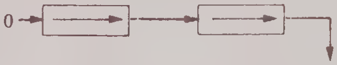
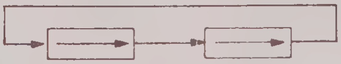
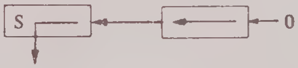
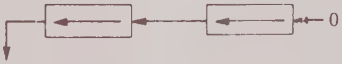
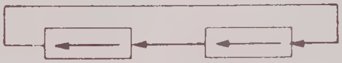
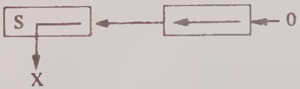
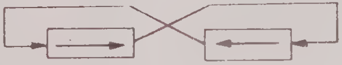
The following paragraphs describe shift full and shift half instructions.

a. *Shift Full (and Double).* Initially, the carry, overflow, and excess indicators are reset. The contents of the process register (H) or the process register pair [illegible] and $(H)_0$ are shifted as specified by the T field of operand (Y), as shown in tables 6-3 and 6-4. The operations of reflect, normalize and shift and count are included as special shift options. On double word shift operations, the leftmost (most significant) word is always contained in an even numbered process register and the rightmost (least significant) word is always contained in an odd numbered process register. In all cases, the H field must be even. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
1A	SHF	Y, H	(H) shifted → H	4.9 + 0.12K

70061-504

Table 6-4. Shift Double Word Instructions

Hex T	Shift Type	Extended Mnemonic*	$(H)_e$ $(H)_o$ Process Register Pair	Comment
08	Algebraic, Right, (Linear), Double Word	SARD		Sign Extended (S = Sign Bit)
0C	Logical, Right, (Linear), Double Word	SLRD		
0D	Circular, Right, Double Word	SCRD		
0A	Algebraic, Left, (Linear), Double Word	SALD		S is not modified
0E	Logical, Left, (Linear), Double Word	SLLD		
0F	Circular, Left, Double Word	SCLD		
1A	Normalize, Double Word	SND		Shift until $X \neq S$ or $K = 0$ K - Shifts ⟶ R
1F	Reflect, Double Word	RFT		

*See the AN/GYK-12 Computer Assembly Language Reference Manual, USACSCS-TF-4-2

70061-16

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
SHF =X'000A',12	Literal	See below.

70061-505

In the above example, the operand looks as follows in binary:

000000000000 1010

The first four bits of the operand specify the R field. It is ZERO, but this option does not use a Tally Register.

The next six bits specify the option. The option is ZERO, which specifies a shift algebraic, right (linear), full word.

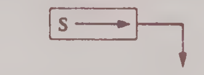
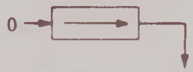
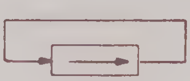
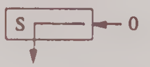
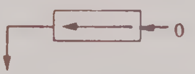
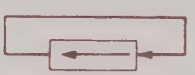
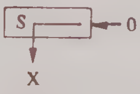
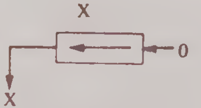
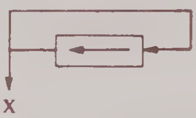
The next six bits specify the number of shifts. The shift count is 10.

It is the content of process register 12 that will be shifted.

Example	Addressing Mode	Action
SHF TPG,11	Direct	The 16 bit content of address TPG is the operand of the instruction. It specifies the R, T and K fields. For full word shift the contents of process register 11 will be shifted. For a double word shift the contents of process registers 10 and 11 will be shifted.

70061-50

Table 6-5. Shift Half Word Instruction

Hex T	Shift Type	Extended Mnemonic*	H_{16-31} Process Register	Comment
00	Algebraic, Right, (Linear), Half Word	SARH		Sign Extended (S = Sign Bit)
04	Logical, Right, (Linear), Half Word	SLRH		
05	Circular, Right, Half Word	SCRH		
02	Algebraic, Left, (Linear), Half Word	SALH		S is not modified
06	Logical, Left, (Linear), Half Word	SLLH		
07	Circular, Left, Half Word	SCLH		
12	Normalize, Half Word	SNH		Shift until X ≠ S or K = 0 K - Shifts ⟶ R
16	Shift and Count, (Linear), Half Word	SCH		Shift until K = 0 Count X = 1's (R(Tally)) + Count ⟶ R
17	Shift and Count, Circular, Half Word	SCCH		Shift until K = 0 Count X = 1's (R(Tally)) + Count ⟶ R

70061-17

*See the AN/GYK-12 Computer Assembly Language Reference Manual, USACSCS-TF-4-2

h. *Shift Half.* Initially, the carry, overflow, and excess indicators are reset. The contents of the process register (H), bit position 16 to 31, are shifted as specified by the T field of the operand (Y), as shown in table 6-5. Bit positions 0 – 15 of (H) are not modified. The operations of normalize and shift and count are included as special shift instructions. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
5A	SHH	Y, H	$(H)_{16\text{-}31}$ shifted $\rightarrow H_{16\text{-}31}$	4.9 + 0.12K

70061-507

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
SHH =0+R'5',14	Literal with indexing	The contents of index register 5 are the actual operand. Bits 16 – 31 of process register 14 are shifted according to the T and K fields of the operand. Bits 0 – 15 of process register 14 are unchanged.

70061-508

Section VI. COMPARE INSTRUCTIONS

6-21. Introduction

The function of these instructions is to compare the contents of full words, half words or parts of words of one register with another register. The comparisons are either algebraic (signed comparisons) or logical (unsigned comparisons). The registers involved in the operations are operand adresses, or operands, and process registers. The end result of the compare instruction is the setting of one of three indicators located in the indicator register: the greater than indicator (OF), the equal indicator (EF) or the less than indicator (LF). Only one of these indicators can be set as the result of an instruction. As an initial action of all compare instructions, the three indicators are reset.

6-22. Instructions

There are eleven instructions in the compare class.

a. *Compare Algebraic Full.* Initially, the carry, greater (overflow), equal, and less indicators are reset. The algebraic value of the operand (Y) is compared with the process register (H). (Y) and (H) are left unchanged. In mode 0, the CA operand is sign extended. If (Y) is greater/equal/less than (H), then the greater/equal/less indicator, respectively is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
10	CMF	Y, H	(Y) : (H) → Ind'r	4.7

70061-509

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Negative word overflow sets the less indicator, and positive word overflow sets the greater indicator.

Example	Addressing Mode	Action
CMF =X'FF'+R'6',9	Literal with indexing	The sign extended hex literal, modified by index register 6, is algebraically compared with the contents of process register 9. If the literal is greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-510

b. *Compare Algebraic Half.* Initially the carry, greater (overflow), equal, and less indicators are reset. The algebraic value of the operand (Y) with extended sign is compared with process register (H). (Y) and (H) are left unchanged. In mode 0, the CA operand is sign extended. If (Y) is greater/equal/less than (H), then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
50	CMH	Y, H	$(Y)_S$: (H) → Ind'r	4.7

70061-619

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Negative word overflow sets the less indicator, positive word overflow sets the greater indicator.

Example	Addressing Mode	Action
CMH (XY+R'5'), 9	Indirect with indexing	The address XY, modified by index register 5, contains a second address. The sign extended contents of the second address are algebraically compared to the contents of process register 9. If the contents of the second address are greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-511

c. *Compare Logical Upper Byte.* Initially, the carry, greater (overflow), equal, and less indicators are reset. The unsigned magnitude of the upper byte of the operand $(Y)_u$ is compared with the unsigned magnitude of bits 24 thru 31 of process register (H). (Y) and (H) are left unchanged. In mode 0, bits 16 thru 23 of CA operand are used. If $(Y)_u$ is greater/equal/less than (H), then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

tion Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
11	CLU	Y, H	$(Y)_U$: $(H)_{24\text{-}31}$ → Ind'r	4.8

70061-512

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Carry out of the bit position 24 affects $(Y)_u$.

Example	Addressing Mode	Action
CLU $+4+R'1',10	Relative with indexing	The effective address is the ILR + 4 + the contents of index register 1. The contents of the upper byte of the effective address are logically compared with the contents of bits 24-31 of process register 10. If the upper byte is greater, the OF indicator is set; if the bytes are equal, the EF indicator is set; if the upper byte is less, the LF indicator is set.

70061-513

d. *Compare Logical Lower Byte.* Initially, the carry, greater (overflow), equal, and less indicators are reset. The unsigned magnitude of the lower byte of the operand $(Y)_L$ is compared with the unsigned magnitude of bits 24 thru 31 of process register (H). (Y) and (H) are left unchanged. In mode 0, bits 24 thru 31 of the CA operand are used. If $(Y)_L$ is greater/equal/less than (H), than the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
51	CLL	Y, H	$(Y)_L$: $(H)_{24\text{-}31}$ → Ind'r	4.8

70061-514

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word position sets the carry indicator. Carry out of the 24 is discarded.

Example	Addressing Mode	Action
CLL =0'377',8	Literal	The lower byte of the octal literal is logically compared to the contents of bits 24-31 of process register 8. If the byte is greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-515

e. *Compare Logical Full.* Initially, the carry, greater (overflow), equal, and less indicators are reset. The 32 bit unsigned (logical) quantity) of the operand (Y) is compared with the 32 bit unsigned quantity of process register (H). (Y) and (H) are left unchanged. In mode 0, the CA operand is zero extended. If (Y) is greater/equal/less than (H), then the greater/equal/less indicator, respectively is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
12	CLF	Y, H	(Y) : (H) → Ind'r	4.8

70061-516

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator.

Example	Addressing Mode	Action
CLF MODE,15	Direct	The contents of address MODE are logically compared with the contents of process register 15. If the contents of MODE are greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-517

f. *Compare Logical Half.* Initially, the carry, greater (overflow), equal, and less indicators are reset. The 16 bit unsigned quantity of the operand (Y) is compared with the 16 bit unsigned quantity of bits 16 thru 31 of process register (H). (Y) and (H) are left unchanged. In mode 0, the CA operand is zero extended. If (Y) is greater/equal/less than (H), then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
52	CLH	Y, H	$(Y) : (H)_{16-31} \rightarrow$ Ind'r	4.8

70061-518

(1) All address modes are permitted.

(2) Special Addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. The least significant 16 bits are compared with the least significant 16 bits of (H).

Example	Addressing Mode	Action
CLH ART- $,11	Relative	The effective address is ART minus ILR. The 16 bit content of the effective address is logically compared with the contents of bits 16-31 of process register 11. If the contents of the effective address are greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-519

g. *Compare Selective Full.* Initially, the carry, greater (overflow), equal, and less indicators are reset. Process register 14 contains a mask. The operand (Y) is logically compared with process register (H) in only those bit positions selected by a ONE in the corresponding bit positions of process register 14. Bit positions in (Y) and (H) are ignored in those bit positions selected by a ZERO in the corresponding bit position in process register 14. In mode 0, the CA operand is zero extended. If the selected field of (Y) is greater/equal/less than the selected field of (H), then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
14	CSF	Y, H	$(Y) \wedge (R_{14})$: $(H) \wedge (R_{14})$ $\rightarrow$ Ind'r	5.6

70061-520

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator.

Example	Addressing Mode	Action
CSF BLW,12	Direct	Logically compares a field of bits in address BLW with a field of bits in process register 12. The field of bits to be compared is determined by the contents of the mask register (process register 14). If the field of bits in BLW is greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set. See the illustration below.

70061-521

(Process Register 14) = 00000000000011111111111100000000

(Process Register 12) = 11111111001000000111010011110001

(BLW) = 00000000001000000111010111100011

comparison made
in these bit
positions only

70061-522

The field of bits in BLW is greater than the field of bits in process register 12. The OF indicator will be set.

h. *Compare Selective Half.* Initially, the carry, greater (overflow), equal, and less indicators are reset. Process register 14 contains a mask. The operand (Y) is logically compared with bit positions 16 thru 31 of process register (H) in only those bit positions selected by a ONE in the corresponding bit position of process register 14. Bit positions in (Y) and (H) are ignored in those bit positions designated by a ZERO in corresponding bit positions in process register 14. In mode 0, the CA operand is zero extended. If the selected field of (Y) is greater/equal/less than the selected field of (H), then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
54	CSH	Y, H	$(Y) \wedge (R_{14})$: $(H)_{16\ 31} \wedge (R_{14})$ $\rightarrow$ Ind'r	5.6

70061-523

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. The masked least significant 16 bits are compared with the masked least significant 16 bits of (H).

Example	Addressing Mode	Action
CSH =X'350',13	Literal	Logically compares a field of bits in the hex literal with a field of bits in bit positions 16-31 of process register 13. The field of bits to be compared is determined by the contents of process register 14. If the field of the literal is greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-524

i. *Compare Gated Full.* Initially, the carry, greater (overflow), equal, and less indicators are reset. Process register 14 must contain a positive number. The absolute value of the algebraic difference between the operand (Y) and process register (H) is compared against the contents of process register 14. In mode 0, the CA operand is sign extended. If the absolute value of the difference is greater/equal/less than contents of process register 14, then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
13	CGF	Y, H	$\|(Y) - (H)\| : (R_{14}) \rightarrow$ Ind'r	5.4

70061-525

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out at the word sign position sets the carry indicator. The greater indicator is set when $(Y)_s - (H)$ overflows.

Example	Addressing Mode	Action
CGF RGHT,4	Direct	In an internal adder, the contents of process register 4 are subtracted from the contents of address RGHT. The absolute value of the difference is compared with the contents of process register 14. If the absolute difference is greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

24

70061-526

j. *Compare Gated Half.* Initially, the carry, greater (overflow), equal, and less indicators are reset. Process register 14 must contain a positive number. The absolute value of the algebraic difference between the operand (Y) with extended sign and process register (H) is compared against the contents of process register 14. In mode 0, the CA operand is sign extended. If the absolute value of the difference is greater/equal/less than contents of process register 14, then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
53	CGH	Y, H	$\|(Y)_S - (H)\| : (R_{14}) \rightarrow$ Ind'r	5.4

70061-527

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out at the word sign position sets the carry indicator. The greater indicator is set when $(Y)_s - (H)$ overflows.

Example	Addressing Mode	Action
CGH =X'F00F',7	Literal	The contents of process register 7 are subtracted from the sign extended hex literal. The absolute value of the difference is compared with the contents of process register 14. If the absolute difference is greater, the OF indicator is set; if equal, the EF indicator is set; if less, the LF indicator is set.

70061-528

k. *Modify and Test Half.* Initially the carry, greater (overflow), equal, and less indicators are reset. The H field of the instruction is used as a signed 4-bit operand. The most significant bit of H is extended as a sign bit. This quantity is added to the half word operand (Y). Bits 16 – 31 of the sum replace Y. The carry indicator is set by half word excess. If the half word sum is positive/zero/negative then the greater/equal/less indicator, respectively, is set. Only one indicator other than the carry is set. The table below illustrates all the possible values for the H field. Trap on carry indicator occurs only when OT indicator is zero.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
6F	MTH	Y,H	(Y) + H→Y ; (Y) : 0→Ind'r	4.8

70061-529

Signed Values of H		
Value of H	Binary Equivalent	Signed Value
H = 0	0000	+0
H = 1	0001	+1
H = 2	0010	+2
H = 3	0011	+3
H = 4	0100	+4
H = 5	0101	+5
H = 6	0110	+6
H = 7	0111	+7
H = 8	1000	-8
H = 9	1001	-7
H = 10	1010	-6
H = 11	1011	-5
H = 12	1100	-4
H = 13	1101	-3
H = 14	1110	-2
H = 15	1111	-1

70061-530

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

NOTE

This instruction allows modification of a half word by any number in the range − 8 thru +7, followed by a test. If the H field is zero, then the specified half word is tested for positive, zero, or negative value.

Example	Addressing Mode	Action
MTH $−21, 10	Relative	The effective address is the ILR-21. The 16 bit content of the effective address is added to the sign extended value -6 (H = 10 is -6) and the result is stored in the effective address. This value is then compared to zero. If greater than zero, the OF indicator is set; if equal to zero, the EF indicator is set; if less than zero, the LF indicator is set.

70061-531

Section VII. LOGIC INSTRUCTIONS

6-23. Introduction

Logic instructions perform logical functions as opposed to arithmetic functions. All values involved in logic operations are assumed to be unsigned quantities, being neither positive or negative, with the sign bit position treated as another magnitude bit. There are three basic operations carried out by the logic instructions. These are Inclusive OR (sometimes referred to as logical sum, union, unite or V), Exclusive OR (sometimes referred to as the modulo two sum, ⊕, or ∀) and AND operations (sometimes referred to as logical product, extract, intersection, or Λ). Corresponding bit positions in the two operands are operated on independently of the other bit positions.

6-24. Inclusive OR Operations

The Inclusive OR operations work with two values, bit position by bit position. For each bit position in the two values, a ONE or a ONE results in a ONE. There is never any carry from one bit position to another.

EXAMPLE: An Inclusive OR operation is performed on the following two values:

```
        1100110011
        0110011001
result  1110111011
```

he following combinations result in a ONE for a given it position:

1 1 0
1 0 1

The following combination results in a ZERO for a given bit position:

0
0

70061-1006

6-25. Exclusive OR Operations

The Exclusive OR operations work with two values, bit position by bit position. For each bit position in the two values a ONE ZERO combination or a ZERO ONE combination results in a ONE. The other combinations result in a ZERO. There is never any carry from one bit position to another.

EXAMPLE: An Exclusive OR operation is performed on the following two values:

1100110011
0110011001
result 1010101010

e following combinations result in a ONE for a given bit sition:

1 0
0 1

The following combinations result in a ZERO for a given bit position:

1 0
1 0

70061-1007

6-26. AND Operations

AND operations work with two values, bit position by bit position. For each bit position in the two values, a ONE ONE combination results in a ONE. All other combinations result in a ZERO. There is never any carry from one bit position to another.

EXAMPLE: An AND operation is performed on the following two values:

1100110011
0110011001
result 0100010001

The following combination results in a ONE for a given bit position:

1
1

The following combinations result in a ZERO for a given bit position:

1 0 0
0 1 0

70061-1008

6-27. Instruction Usages

The logic operations are particularly useful in masking (AND), extracting (AND), inserting (OR) and complementing (Exclusive OR) functions. They are also useful in testing and nonequivalence (Exclusive OR) operations. The operations can involve a single bit or a field of bits within a full or half word.

6-28. Instructions

The logic instructions are described in the following paragraphs.

a. *Inclusive OR Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically merged with the process register (H). For every ONE bit in (Y) a ONE is inserted into that bit position of (H), regardless of its original state. ZERO bits in (Y) do not modify the corresponding bit position in (H). The result replaces H. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
15	IOF	Y, H	(H) ∨ (Y) → H	4.7

70061-532

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
IOF ZBTA,9	Direct	An Inclusive OR is performed between the contents of address ZBTA and process register 9 with the results stored in process register 9.

70061-533

b. *Inclusive OR Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically merged with the least significant 16 bits of the process register (H). For every (Y), a ONE bit in (Y), a ONE is inserted into that bit position of (H), regardless of its original state. ZERO bits in (Y) do not modify the corresponding bit position in (H). The result replaces bits 16 – 31 of H; bits 0 – 15 of (H) are not changed. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
55	IOH	Y, H	$(H)_{16-31} \vee (Y) \rightarrow H_{16\ 31}$	4.7

70061-534

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
IOH =0'7777',8	Literal	An Inclusive OR is performed between the octal literal and the contents of bits 16 31 of process register 8. The result is stored in bits 16 31 of process register 8 with bits 0 15 remaining unchanged.

70061-535

c. *Replace Inclusive OR Full.* Indicators are not affected. Process register (H) is logically merged with the operand (Y). For every ONE bit in (H), the corresponding bit position of (Y) is set to a ONE regardless of its original state. For every ZERO bit in (H), the corresponding bit position of (Y) is not changed. The result replaces Y. (H) is not changed. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
ID	RIF	Y, H	$(Y) \vee (H) \rightarrow Y$	5.1

70061-536

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RIF FYI+R'2',11	Direct with indexing	An Inclusive OR is performed between the contents of the modified address FYI and process register 11 with the results stored in the modified address FYI.

70061-537

d. *Replace Inclusive OR Half.* Indicators are not affected. The least significant 16 bits at process register (H) are logically merged with the operand (Y). For every ONE bit in (H), the corresponding bit position (Y) is set to a ONE regardless of its original state. For every ZERO bit in (H), the corresponding bit position of (Y) is not changed. Bits 16 – 31 of the result replace Y. (H) is not changed. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
5D	RIH	Y, H	$(Y) \vee (H)_{16\ 31} \rightarrow Y$	5.1

70061-538

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RIH $+12+R'1'.3	Relative with indexing	The effective address is the ILR + 12 + the contents of index register 1. An inclusive OR is performed between the contents of the effective address and process register 3 with bits 16 – 31 of the result stored in the effective address.

70061-539

e. *Exclusive OR Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically matched with the process register (H). For every ONE bit in (Y) and corresponding ZERO bit in (H), a ONE is inserted into that bit position of (H). For every ONE bit in (Y) and corresponding ONE bit in (H), a ZERO is inserted into that bit position of (H). ZERO bits in (Y) do not modify the corresponding bit positions in (H). The result replaces H. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
16	EOF	Y, H	$(H) \forall (Y) \rightarrow H$	4.7

70061-540

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
EOF (HOPP),15	Indirect	The contents of address HOPP are a second address. An exclusive OR is performed between the contents of the second address and process register 15 with the result stored in process register 15.

70061-541

f. *Exclusive OR Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically matched with the least significant 16 bits of the process register (H). For every ONE bit in (Y) and corresponding ZERO bit in (H), a ONE is inserted into that bit position of (H). For every ONE bit in (Y) and corresponding ONE bit in (H), a ZERO is inserted into that bit position of (H). ZERO bits in (Y) do not modify the corresponding bit positions in (H). The result replaces bits 16 – 31 of H; bits 0 – 15 of (H) are not changed. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
56	EOH	Y, H	$(H)_{16\text{-}31} \forall (Y) \rightarrow H_{16\text{-}31}$	4.7

70061-542

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
EOH *+13,12	Direct	The effective address is the instruction address +13. An exclusive OR is performed between the contents of the effective address and bits 16 – 31 of process register 12 with the result stored in bits 16 – 31 of process register 12.

70061-543

g. *Replace Exclusive OR Full.* Indicators are not affected. Process register (H) is logically matched with operand (Y). For every ONE bit in (H), the corresponding bit position of (Y) is set to a ONE if it was a ZERO or it is reset to a ZERO if it was a ONE. ZERO bits in (H) will not change the corresponding bit positions in (Y). (H) is not changed. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
1E	REF	Y, H	$(Y) \forall (H) \rightarrow Y$	4.7

70061-544

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
REF MT+D'4',14	Direct with double indexing	The effective address is MT as modified by the contents of index registers 1 and 4. An exclusive OR is performed between the contents of the effective address and process register 14. The result is stored in the effective address.

70061-545

h. *Replace Exclusive OR Half.* Indicators are not affected. The least significant 16 bits of process register (H) are logically matched with the operand (Y). For every ONE bit in (H), the corresponding bit position of (Y) is set to a ONE if it was a ZERO or it is reset if it was a ONE. ZERO bits in (H) will not change the corresponding bit positions in (Y). Bits 16 – 31 of the result replace Y. (H) is not changed. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
5E	REH	Y, H	$(Y) \forall (H)_{16\ 31} \rightarrow Y$	5.1

70061-546

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
REH (DPL+R'7'),8	Indirect with indexing	The modified address DPL contains a second address. An exclusive OR is performed between the contents of the effective address and process register 8. Bits 16 - 31 of the result are stored in the effective address.

70061-547

i. *Logical AND Full.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically masked with the process register (H). For each ZERO bit in (Y), the corresponding bit position in (H) is reset to a ZERO. For each ONE bit in (Y), the corresponding bit position in (H) remains unchanged. The result replaces H. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
17	ANF	Y, H	$(H) \wedge (Y) \rightarrow H$	4.7

70061-548

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
ANF =X'C'+R'3',9	Literal with indexing	An AND operation is performed between the modified hex literal (zero extended) and the contents of process register 9 with the result stored in process register 9.

70061-549

j. *Logical AND Half.* Initially, the carry, overflow, and excess indicators are reset. The operand (Y) is logically masked with the least significant 16 bits of the process register (H). For each ZERO bit in (Y), the corresponding bit position in (H) is reset to a ZERO. For each one-bit in (Y), the corresponding bit position in (H) remains unchanged. The result replaces bits 16 – 31 of H; bits 0 – 15 of H are not changed. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
57	ANH	Y, H	$(H)_{16\ 31} \wedge (Y) \rightarrow H_{16\ 31}$	4.7

70061-550

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
ANH $ 9,13	Relative	The effective address is ILR -9. An AND operation is perfromed on the contents of the effective address and bits 16 - 31 of process register 13. The result is stored in bits 16 - 31 of process register 13 with bits 0 - 15 remaining unchanged.

70061-551

k. *Replace Logical AND Full.* Indicators are not affected. Process register (H) is logically masked with the operand (Y). For every ONE bit in (H), the corresponding bit position in (Y) is not changed. For every ZERO bit in (H), the corresponding bit position in (Y) is reset to a ZERO. The result replaces Y. (H) is not changed. Indicators are not modified. Trap never occurs.

c-tion Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
1F	RNF	Y, H	$(Y) \wedge (H) \rightarrow Y$	5.1

70061-552

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RNF MU,1	Direct	An AND operation is performed between the contents of address MU and process register 1 with the result stored in address MU.

70061-553

l. *Replace Logical AND Half.* Indicators are not affected. The least significant 16 bits of process register (H) are logically masked with the operand (Y). For every ONE bit in (H), the corresponding bit position in (Y) is not changed. For every ZERO bit in (H), the corresponding bit position in (Y) is reset to a ZERO. Bits 16 – 31 of the result replace Y. (H) is not changed. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
5F	RNH	Y, H	$(Y) \wedge (H)_{16\text{-}31} \rightarrow Y$	5.1

70061-554

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
RNH (ALTA),6	Indirect	The contents of ALTA are a second address. An AND operation is performed between the contents of the second address and process register 6. Bits 16 – 31 of the result are stored in the second address.

70061-555

m. *Selective Substitute Full.* Indicators are not affected. Process register 14 contains a mask. The instruction stores the contents of the process register (H) in the operand location (Y) in those bit positions selected by a ONE in corresponding bit positions of process register 14. The operand (Y) remains unchanged in those bit positions selected by a ZERO in corresponding bit positions of process register 14. (H) is not changed. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
2F	SSF	Y, H	$[(H) \wedge (R_{14})] \vee [(Y) \wedge (\overline{R_{14}})] \rightarrow Y$	5.7

70061-556

(1) Address mode 0 is excluded.

(2) Special addresses: process registers only.

Example	Addressing Mode	Action
SSF RES,10	Direct	The contents of process register 10 are stored in address RES in those bit positions selected by a 1 in corresponding bit positions within the mask register (process register 14). See the example below.

Before:

```
(Process
Register 14)  =  00000000000|11111|0000000000000000

(Process
Register 10)  =  11000011101|01100|0011001000111011

(RES)         =  00010001101|01011|0110000000001110

After: (RES)  =  00010001101|01100|0110000000001110
                 |<-no change->|<-insert->|<-no change->|
```

70061-557

Section VIII. BIT INSTRUCTIONS

6-29. Introduction

The basic function of the set/reset instructions is to set a bit within a half word to a ONE or to reset a bit in a half word to ZERO. The basic function of the test instructions is to test a bit within a half word and, based upon the results of the test, to either execute the next instruction in sequence (mismatch) or skip the next instruction in sequence (match).

6-30. Bit Instructions

Set/reset and test instructions are described in the following paragraphs.

a. *Set Bit in Half Word.* Indicators are not affected. The H-field specifies a bit position (0 to 15 or 16 to 31) within the half word operand (Y) that will be set to a ONE. Other bits of (Y) are not changed. If the program activity register is addressed, a program level change is not attempted. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
1C	SBT	Y, H	$1 \rightarrow (Y)_i \; 0 \leq i \leq 15$	5.0

70061-558

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
SBT LTI+R'2',1	Direct with indexing	Bit position ONE within the modified address LTI is set to a ONE. The other bit positions within the half word are not disturbed.

70061-559

b. *Reset Bit in Half Word.* Indicators are not affected. The H-field specifies a bit position (0 to 15 or 16 to 31) within the half word operand (Y) that will be reset to a ZERO. Other bits of (Y) are not changed. If the program activity register is addressed, a program level change is not attempted. Indicators are not modified. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
5C	RBT	Y, H	$0 \rightarrow (Y)_i \; 0 \leq i \leq 15$	5.0

70061-560

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9.

Example	Addressing Mode	Action
RBT $ 11,8	Relative	The effective half word address is the ILR-11. Bit position 8 within the effective address is reset to ZERO. The other bit positions within the half word are not disturbed.

70061-561

c. *Test Bit in Half Word for ZERO, Skip on Match.* Indicators are not affected. The H field specifies a bit position (0 to 15 or 16 to 31) within the half word operand (Y) to be tested. If the bit tested is a ZERO, then the next instruction in sequence is skipped. If the bit tested is a ONE, then the next instruction in sequence is obtained. (H) and (Y) are not changed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
37	TSZ	Y, H	If $(Y)_i = 0$ $(ILR)+2 \rightarrow ILR$; If $(Y)_i \neq 0$ No operation $0 \leq i \leq 15$	4.8

70061-562

(1) Address mode 0 is excluded.

(2) Special addresses: all, see tables 6-2 and 6-9 (privilege not required).

Example	Addressing Mode	Action
TSZ (ZEST),15	Indirect	The contents of ZEST are a second address. Bit 15 of the contents of the second address is tested. If it is a ZERO the next instruction in sequence is skipped. If it is a ONE the next instruction in sequence is executed.

70061-563

d. *Test Bit in Half Word for ONE, Skip on Match.* Indicators are not affected. The H field specifies a bit position (0 to 15 or 16 to 31) within the half word operand (Y) to be tested. If the bit tested is a ONE then the next instruction in sequence is skipped. If the bit tested is a ZERO then the next instruction in sequence is obtained. (H) and (Y) are not changed.

[illegible]nction Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
77	TSO	Y, H	If $(Y)_i = 1$ $(ILR)+2 \rightarrow ILR$; If $(Y)_i \neq 1$ No operation $0 \le i \le 15$	4.8

70061-564

(1) Address mode 0 is excluded.

(2) Special addresses: see tables 6-2 and 6-9 (privilege not required).

Example	Addressing Mode	Action
TSO RBN+R'2',0	Direct with Bit indexing	ZERO of the contents of the modified address RBN is tested. If the bit is a ONE the next instruction in sequence is skipped. If it is a ZERO the next instruction in sequence is executed.

70061-565

e. *Test and Conditionally Insert/Skip.* Indicators are not affected. The half-word operand (Y) is inclusive OR'ed with bits 16 to 31 of process register H and is stored in half word (Y). If half word operand (Y), prior to Inclusive OR operation is ZERO, then the next instruction in sequence is skipped. If the half word operand (Y) is not ZERO, then the next instruction in sequence is obtained. The next instruction is always executed as if the level lock was set for the TSI and following instruction. (The next instruction executed is obtained from (ILR) or (ILR +2).

The test/insert operation is performed in a split memory cycle which is not interruptible.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
76	TSI	Y, H	$(H)_{16\text{-}31} \vee (Y)_{\text{half word}} \rightarrow (Y)_{\text{half word}}$ If $(Y)_{\text{half word}} = \text{Zero}, (ILR) + 2 \rightarrow (ILR)$ If $(Y)_{\text{half word}} \neq \text{Zero}, (ILR) \rightarrow (ILR)$ An interrupt between this instruction and the following instruction is not possible The tests are performed on $(Y)_{\text{half word}}$ before the inclusive "OR" operation takes place	5.3

70061-566

(1) Address mode 0 is excluded.

(2) Special address: Process registers only.

Example	Addressing Mode	Action
TSI ERR,9	Direct	The contents of address ERR is tested for ZERO. If ZERO, the Instruction Location Counter is incremented by 2 to skip the next instruction in sequence. If non-ZERO, the next instruction in sequence will be obeyed. In either case, the half-word contents of address ERR will be inclusively ORed with bits 16-31 of process register 9 and the result placed back in address ERR. This is all done in a split memory cycle and the next instruction will be accessed as if the level lock had been set (either ILR or ILR+2).

70061-567

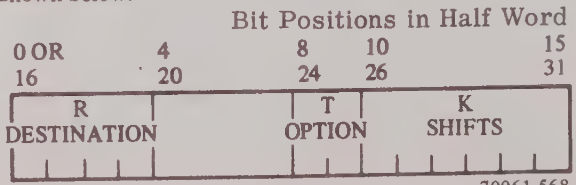
Section IX. FORMAT INSTRUCTIONS

6-31. Introduction

The format instructions serve two basic purposes. One function will extract a field of bits from a process register and isolate that field in a second process register. The other function will extract a field of bits from a process register and insert the extracted field into another process register without disturbing the other bits in the receiving register. Both functions allow for the formatting of the extracted field. The formatting consists of shifting the extracted field of bits, to the left or to the right, a number of specified bit positions.

6-32. The Operand of Format Instructions

Each format instruction requires a 16 bit operand which has three fields. An illustration of the operand is shown below.



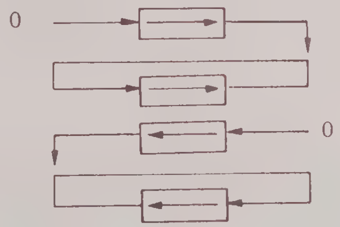
70061-568

a. *R*: This field is four bits in length and occupies the first four bits of the operand. It will contain a number from 0 – 15 which refers to a process register. This process register will receive the results of the operation and is referred to as the destination or TO register.

The next four bits are always blank and have no meaning to the instructions.

b. *T*: The next two bits make up the T field. It specifies one of the four shift options available to the format instructions. The table below illustrates the options.

c. *K*: The last 6 bits specifies the number of bit positions to be shifted in the selected process register (H) prior to its logical operation with the mask contained in process register 14 (R'14'). Any value from 0 to 63 may be specified as a shift count in a single operation. A K field equal to ZERO specifies no shift.

T	Shift Operation	Process Register (H)
0	Right, Linear	
1	Right, Circular	
2	Left, Linear	
3	Left, Circular	

70061-620

6-33. Extended Mnemonics For Format Instructions

The AN/GYK-12 Assembler provides extended mnemonics for each of the format instructions (see table below). There are four extended mnemonics for each instruction, one for each of the available shift options. A detailed discussion of the extended mnemonics for format instructions is provided in the AN/GYK-12 Computer Assembly Language Reference Manual, USACSCS-TF-4-2.

FORMAT EXTRACT

FELRF	Linear, Right, Full Word	T = 0
FECRF	Circular, Right, Full Word	T = 1
FELLF	Linear, Left, Full Word	T = 2
FECLF	Circular, Left, Full Word	T = 3
FELRH	Linear, Right, Half Word	T = 0
FECRH	Circular, Right, Half Word	T = 1
FELLH	Linear, Left, Half Word	T = 2
FECLH	Circular, Left, Half Word	T = 3

FORMAT INSERT

FILRF	Linear, Right, Full Word	T = 0
FICRF	Circular, Right, Full Word	T = 1
FILLF	Linear, Left, Full Word	T = 2
FICLF	Circular, Left, Full Word	T = 3
FILRH	Linear, Right, Half Word	T = 0
FICRH	Circular, Right, Half Word	T = 1
FILLH	Linear, Left, Half Word	T = 2
FICLH	Circular, Left, Half Word	T = 3

70061-621

6-34. Instructions

Format instructions are described in the following paragraphs.

a. *Format Extract Full.* Initially, the carry, overflow, and excess indicators are reset. Process register 14 contains a mask. The contents of the process register (H) are shifted right or left, linear or circular as specified by the T field of the operand (Y). The number of shifts is specified by the K field. The contents of process register 14 contains a mask which is logically ANDed with the shifted word. The result replaces the contents of the process register specified by the R field. The contents of the process register (H) and mask (R_{14}) are not changed. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
18	FEF	Y,H	$[(H)\ \text{shifted}] \wedge (R_{14}) \rightarrow R$	5 3 + 0.12K

70061-569

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
FEE =X'B008',8	Literal	The current contents of Process Registers are as follows (R'8') = 000017A6$_{16}$ 0000000000000000 0010111101001100$_2$ (R'11') = 000084BA$_{16}$ 0000000000000001 0000100101110101$_2$ (R'14') = 0000003E$_{16}$ 0000000000000000 0000000000111110$_2$ The following instruction is executed: FEE = X'B008',8 Process Register which is to receive result R'11' Shift Option Right Linear Number of Shifts 8 The contents of Process Registers after instruction execution (R'8') = 000017A6$_{16}$ (R'11') = 00000016$_{16}$ (R'14') = 0000003E$_{16}$ The operation **The contents of R'8' are shifted in the arithmetic section 8 bit positions to the right, with the least significant 8 bits being lost (linear shift) and zeros filling the vacated bit positions.** Interim Results 0000000000000000 0000000000010111 A logical AND is performed between the shifted quantity and the contents of the Mask Register (R'14') Result 0000000000000000 0000000000010110 The result is stored in the TO (Destination) Process Register (R'11') The contents of R'8' and R'14' remain unchanged.

70061-570

b. *Format Extract Half.* Initially, the carry, overflow, and excess indicators are reset. Process register 14 contains a mask. The contents of the process register (H), bit positions 16 – 31, are shifted right or left, linear or circular as specified by the T field of the operand (Y). The number of shifts is specified by the K field. The contents of process register 14, bit positions 16 – 31, contains a mask which is logically ANDed with the shifted half word. The result replaces the contents of the least significant 16 bits of the process register specified by the R field. The contents of the process register (H), mask (R_{14}), and bits 0 to 15 of (R) are not changed. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
58	FEH	Y,H	$[(H)_{16\text{-}31}$ shifted$]$ $\wedge (R_{14}) \rightarrow R_{16\text{-}31}$	5.3 + 0.12K

70061-571

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
FEH $+R'1',11	Relative with indexing	The effective address of the operand is the ILR+ the contents of index register 1. A field of bits in process register 11 is extracted according to the mask in process register 14. The field is shifted according to the T and K fields of the operand and the result is stored in the destination register specified by the R field of the operand. The extracted field of bits in process register 11 must be between bit positions 16 and 31. Bits 0 – 15 of the destination register remain undisturbed.

70061-572

c. *Format Insert Full.* Initially, the carry, overflow, and excess indicators are reset. Process register 14 contains a mask. The contents of the process register (H) are shifted right or left, linear or circular as specified by the T field of the operand (Y). The number of shifts is specified by the K field. The contents of process register 14 contain a mask which is logically ANDed with the shifted word. The inverted mask (ONE's complement) is logically ANDed with the process register specified by the R field and the resulting quantity is ORed with the shifted, masked word. The result replaces the contents of the process register specified by the R field. The contents of the process register (H) and mask (R_{14}) are not changed. A ONE bit in the mask will reset the corresponding bit position in process register R. It will take the corresponding bit from the shifted process register (H) and insert it into the corresponding bit position in process register R. A ZERO bit in the mask (R_{14}) will not change the corresponding bit position in process register R. In mode 0, the CA operand is ZERO extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
19	FIF	Y, H	$\{[(H)$ shifted$]$ $\wedge (R_{14})\}$ $\vee \{(R) \wedge (\overline{R_{14}})\}$ $\rightarrow R$	5.9 + 0.12K

70061-573

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
FIF =X'C088'.7	Literal	The current contents of process registers are as follows: (R'7') = $004A6710_{16}$ 0000000001001010011 0011100010000_2 (R'12') = $6344AAFC_{16}$ 0110001101000100101 0101011111100_2 (R'14') = $00FFF000_{16}$ $00000000\underline{11111111111}$ $\underline{1}000000000000_2$ The following instruction is executed FIF = X'C088'.7 Process Register which is to receive the result: R'12' Shift Option: Left Linear Number of shifts. 8 The contents of Process Registers after instruction execution The operation: The contents of R'7' are shifted in the arithmetic section 8 bit positions to the left. with the most significant 8 bits being lost (linear shift) and ZERO(s) filling the vacated bit positions Interim Result 1: $01001010\underline{01100111000}$ $4A671000_{16}$ $\underline{1}000000000000_2$ A logical AND is performed between the shifted quantity and the contents of the mask register (R'14'). Interim Result 2: $00000000\underline{01100111000}$ 00671000_{16} $\underline{1}000000000000_2$ In the arithmetic section, the contents of the mask register (R'14') are inverted (ONE's complement). A logical AND is performed between the inverted mask and the contents of the TO (Destination) process register (R'12'). Interim Result 3. $01100011\underline{00000000000}$ $63000AFC_{16}$ $\underline{0}101011111100_2$ A logical inclusive OR is performed between interim result 2 and interim result 3. Result: $01100011\underline{01100111000}$ $63671AFC_{16}$ $\underline{1}101011111100_2$ The result is stored in the TO (Destination) process register (R'12'). The contents of R'7' and R'14' remain unchanged

70061-574

d. *Format Insert Half.* Initially, the carry, overflow, and excess indicators are reset. Process register 14 contains a mask. The contents of the process register (H), bit positions 16 – 31, are shifted right or left, linear or circular as specified by the T field of operand (Y). The number of shifts is specified by the K field. The contents of process register 14, bit positions 16 – 31, contain a mask which is logically ANDed with the shifted half word. The inverted mask (ONE's complement) is logically ANDed with the process register specified in the R field, bit positions 16 – 31, and the resulting quantity is ORed with the shifted, masked half word. The result replaces the contents of the least significant 16 bits of the process register specified by the R field. The contents of the process register (H), mask (R_{14}), and bits 0 to 15 of (R) are not changed. A ONE bit in the mask will reset the corresponding bit position in process register R, bit positions 16 thru 31. It will take the corresponding bit from the shifted process register (H), bit positions 16 to 31, and insert it into the corresponding bit position in process register R. A ZERO bit in the mask (R_{14}) will not change the corresponding bit position in process register R. In mode 0, the CA operand is zero extended. Indicators are set only in mode 0 with indexing. Trap never occurs.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
59	FIH	Y,H	$\{[(H)_{16\text{-}31}\text{ shifted}] \wedge (R_{14})\} \vee \{(R)_{16\text{-}31} \wedge \overline{(R_{14})}\} \rightarrow R_{16\text{-}31}$	5 9 + 0.12K

70061-575

(1) All address modes are permitted.

(2) Special address, process registers only.

(3) Mode 0 with indexing: carry out of the word sign position sets the carry indicator. Word overflow sets the overflow indicator. A sum exceeding a half word sets the excess indicator.

Example	Addressing Mode	Action
FIH LESS, 9	Direct	A field of bits in process register 9 is extracted according to the mask in process register 14. The field is shifted according to the T and K fields contained in the operand address LESS and the result is stored in the destination register specified by the R field of the operand. The extracted field of bits in process register 9 must be between bit positions 16 and 31. Bits 0 – 15 of the destination register remain undisturbed. Only those bit positions between 16 and 31 of the destination register are changed which correspond to one bits in process register 14.

70061-576

Section X. PROGRAM LEVEL TRANSFER INSTRUCTIONS

6-35. Introduction

The function of these instructions is to call other program modules by changing program levels. To effect this change of program levels, the instructions set and reset information into some of the special registers of the AN/GYK-12 Computer. Some of the special registers involved are the privilege and level link register, the executive link register, the program activity register, the query register and the queue register.

6-36. Instructions

The following paragraphs describe program level transfer instructions:

a. *Call Executive Program Level and Link.* Indicators are not affected. The operand (Y) is inserted into the argument field A of the privilege and level link word corresponding to the level specified by the executive program level XPL field of the executive link register. The active program level (APL) is inserted into the link program level (LPL) field of the privilege and level link word corresponding to the XPL of the executive-link register. The status bit PS in the program activity register correponsing to the program level specified by the XPL field of the executive link register is set to a ONE. The status bit PS corresponding to the APL is reset when the most significant bit of the (Y) operand is ZERO. The second and third bit of the (Y) operand must be ZERO. The Program Level Lock is set. Process register 0 only is saved when the LC indicator is set. If not set, save all process registers. A program level change to the executive program level XPL takes place. Registers are loaded according to the C field of the privilege and level link register of the executive program level. Note that when bit position 9 of the C field is ONE, then an access of page control and address registers 4 thru 15 will be treated as an access violation.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
3C	TXP	Y	See the following	30-150

70061-577

(Y) → (A field of privilege and level link word)$_{XPL}$

APL → (LPL field of privilege and level link word)$_{XPL}$

1 → (PS of Program Activity Register)$_{XPL}$

0 → (PS of Program Acitivity Register)$_{APL}$ if (Y)$_0$ = 0

1 → Program Level Lock

If LC = 1, save Process Register 0 only, Level change to Executive Program Level.

70061-578

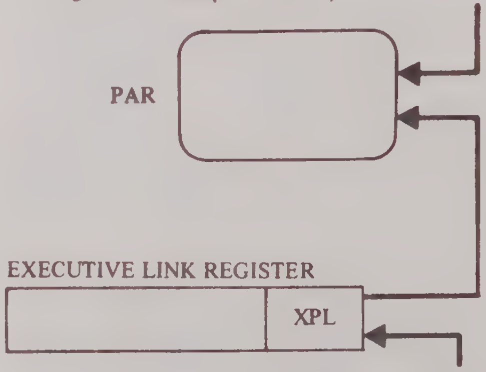
(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

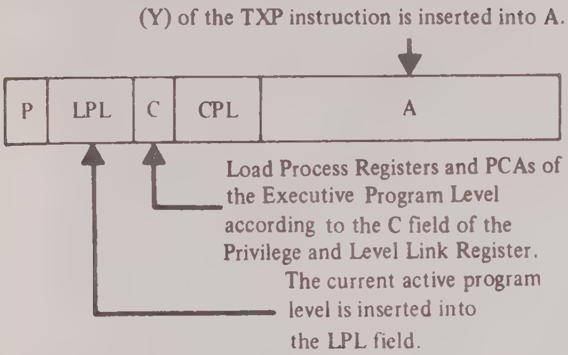
Example	Addressing Mode	Action
TXP =0	Literal	See below.

If (Y)$_0$ = 0 reset status bit of current active program (sign bit in example is ZERO).



Set status bit of Executive Program Level to ONE in the PAR (XPL field contains level of the Executive).

PRIVILEGE AND LEVEL LINK REGISTER OF CALLED PROGRAM LEVEL


(Y) of the TXP instruction is inserted into A.
P
LPL
C
CPL
A
Load Process Registers and PCAs of the Executive Program Level according to the C field of the Privilege and Level Link Register.
The current active program level is inserted into the LPL field.

Additionally:

Before the program level change the contents of the Process Registers of the current active program level are stored according to the setting of the Level Change Indicator (LC) in the Indicator Register, the Level Lock Indicator (LLI) in the Query Register is set to ONE as a result of this instruction.

70061-581

b. *Call Program Level and Link.* Indicators are not affected. When the second bit in the operand $(Y)_1$ is a ZERO, then the called program level (CPL) is specified by the CPL field of the privilege and level link register. When this bit $(Y)_1$ is a ONE, the program level 63 will be called. The operand (Y) is inserted into the argument field A of the privilege and level link word corresponding to the level called. The active program level (APL) is inserted into the link program level field (LPL) of the privilege and level link word corresponding to the level called. The status bit PS in the program activity register corresponding to the level called is set to a ONE. The status bit PS in the program activity register corresponding to the APL is reset when the most significant bit of the $(Y)_0$ operand is ZERO. When the third bit $(Y)_2$ in the operand is a ONE, then a bit in the Queue word corresponding to the called program level (CPL or 63 depending upon the (Y) option) is set to a ONE. The operand bit positions $(Y)_{3\text{-}7}$ specify a bit position 0 to 31 within the Queue word that will be set to a ONE. Other bits in the Queue word are not changed. The Program Level lock is reset. Process register 0 only is saved when the LC indicator is set. If not set, save all process registers. A program level change is attempted at the conclusion of the instruction by auction. Registers are loaded according to the C field in the privilege and level link register of the program level determined by the program level change. Note that when bit position 9 of the C field is ONE, then an access of page control and address registers 4 thru 15 are treated as a memory access violation.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
7C	TCP	Y	See the following	30-150

70061-582

$(Y)_1$ = 0 use CPL

$(Y)_1$ = 1 use level 63

(Y) → (A field of privilege and level link word)$_{CPL/level}$

APL → (LPL field of privilege and level link word)$_{CPL/level\ 63}$

1 → (PS of Program Activity Register)$_{CPL/level\ 63}$

0 → (PS of Program Activity Register)$_{APL}$ if $(Y)_0 = 0$

Set ith bit in (Queue Word)$_{CPL/level\ 63}$ if $(Y)_2 = 1$

i = $(Y)_{3\text{-}7}$

0 → Program Level Lock.

If LC = 1, save Process Register 0 only.

Attempt level change by auction.

70061-583

(1) All address modes are permitted.

(2) Special addresses: process registers only.

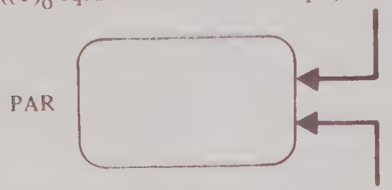
(3) Mode 0 with indexing: carry out of the half word sign position is discarded:

NOTE

Registers are always swapped. The PPL (Prior Program Level) field in the query register will contain the program level number of this program level even when the attempted program level change results in the program level which executed this called program level and link instruction. This instruction actually causes an 'auction' to occur. That is, a scan of the program activity register is begun from the highest program level to the lowest. The highest priority program level, with program status and program enable bits both set to one, is the program level which is activated. This may not be the CPL indicated by this instruction if a higher level has both bits set to ONE.

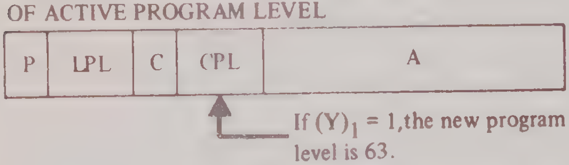
Example	Addressing Mode	Action
TCP =X'2100'	Literal	See below

If $(Y)_0 = 0$ reset status bit of current active program level (($(Y)_0$ equals ZERO in the example).



The status bit of the called program level is set to ONE.

PRIVILEGE AND LEVEL LINK REGISTER OF ACTIVE PROGRAM LEVEL

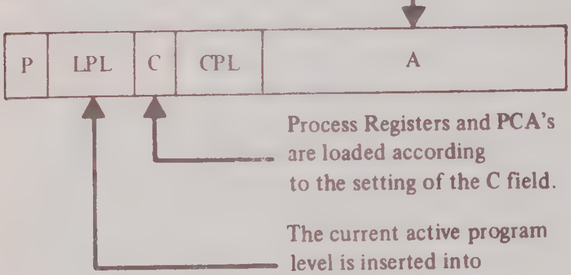


If $(Y)_1 = 1$, the new program level is 63.

If $(Y)_1 = 0$ the new program level is specified by the CPL field (($(Y)_1$ equals ZERO in the example).

PRIVILEGE AND LEVEL LINK REGISTER OF CALLED PROGRAM LEVEL

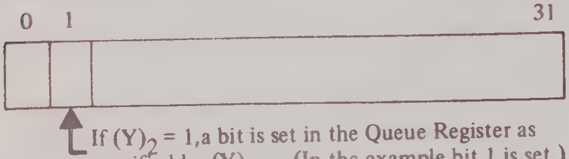
The operand is inserted into the A field.



Process Registers and PCA's are loaded according to the setting of the C field.

The current active program level is inserted into the LPL field.

QUEUE REGISTER



If $(Y)_2 = 1$, a bit is set in the Queue Register as specified by $(Y)_{3-7}$. (In the example, bit 1 is set.)

Additionally:

The contents of Process Registers of the current active program level are stored according to the setting of the Level Change Indicator (LC) in the Indicator Register.

The Level Lock Indicator (LLI) in the Query Register is reset to ZERO as a result of this instruction.

70061-584

c. *Tie Program Level and Link (Semiprivileged).* Indicators are not affected. The operand (Y) is inserted into the argument field A of the privilege and level link word corresponding to the level specified by the call program level (CPL) field of the privilege and level link register. The second and third bit of the (Y) operand must be ZERO. The active program level (APL) is inserted into the link program level field LPL of the privilege and level link word corresponding to CPL of the privilege and level link register. The status bit PS in the program activity register corresponding to the APL is reset when the most significant bit of the (Y) operand is ZERO. The status bit PS in the program activity register corresponding to the level specified by the CPL field of the privilege and level link register is set to a ONE. Save only process register 0 if LC = 1, otherwise save all process registers, level change to tie program level. The Program Level Lock is Set. Process register 0 only is saved when the LC indicator is set. If not set, save all process registers. A program level change to the tie program level CPL takes place. Registers are loaded according to the C field in the privilege and level link register of the tied program level with the following exception. Note that when bit position 9 of the C field is ONE, an access of page control and address registers 4 thru 15 will be treated as an access violation.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
3D	TIE	Y	See Below	30-150

70061-587

$(Y) \rightarrow$ (A field of privilege and level link word)$_{CPL}$

APL $\rightarrow$ (LPL field of privilege and level link word)$_{CPL}$

$0 \rightarrow$ (PS of Program Activity Register)$_{APL}$ if $(Y)_0 = 0$

$1 \rightarrow$ (PS of Program Activity Register)$_{CPL}$

$1 \rightarrow$ Program Level Lock.

If LC = 1, save Process Register 0 only, Level change to Tie Program Level

70061-588

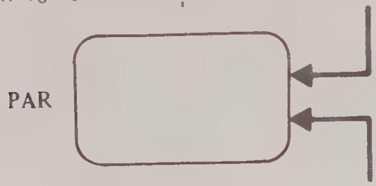
(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: Carry out of the half word sign position is discarded.

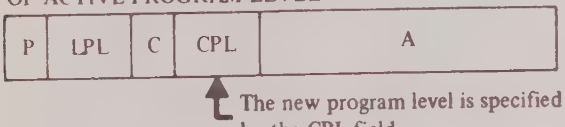
Example	Addressing Mode	Action
TIE = X'8000'	Literal	See below.

If $(Y)_0$ = 0 reset status bit of current active program level ($(Y)_0$ equals ONE in the example).



The status bit of the called program level is set to ONE.

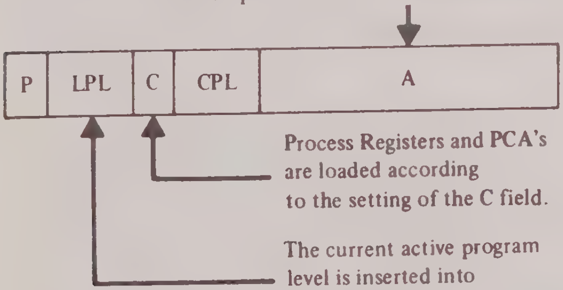
PRIVILEGE AND LEVEL LINK REGISTER
OF ACTIVE PROGRAM LEVEL



The new program level is specified by the CPL field.

PRIVILEGE AND LEVEL LINK REGISTER
OF CALLED PROGRAM LEVEL

The operand is inserted into the A field.



Process Registers and PCA's are loaded according to the setting of the C field.

The current active program level is inserted into the LPL field.

Additionally:

The contents of Process Registers of the current active program level are stored according to the setting of the Level Change Indicator (LC) in the Indicator Register.

The Level Lock Indicator (LLI) in the Query Register is set to one as a result of this instruction.

70061-589

d. *Test and Conditionally Reset/Skip.* Indicators are not affected. When the operand address Y specifies a process register (0 to $1F_{16}$) or the Queue Register (32_{16}), then the 32 bit register is tested. If the register is not ZERO, then the most significant non-ZERO bit position is translated into a bit position number which is stored in process register H bits (27 – 31). Bits (0 – 26) set to ZERO. The bit position is reset and the next instruction in sequence is skipped. If the register is ZERO, process register H is not changed and the instruction location register refers to the next instruction in sequence. The status bit PS in the program activity register corresponding to the active program level (APL) is reset. The program level lock is reset. Process register 0 only is saved when the LC indicator is set. If not set, save all process registers. A program level change is attempted. When the operand address Y specifies a memory location ($\geq 40_{16}$), then the memory word is tested. If the word is not ZERO, then the most significant non ZERO bit position is translated into a bit position number which is stored in process register H. The bit position is reset to zero and the next instruction in sequence is skipped. If the contents of the memory location is ZERO, process register H is not changed and the next instruction in sequence is obtained. The most significant tested bit position corresponds to 0; the least significant bit position to $1F_{16}$. This number replaces the contents of the least significant five bits (27 to 31) of process register (H). Bit 0 to 26 of (H) are set to ZERO.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
5B	TQR	Y, H	See Below	6-150

If Y = 0 to $1F_{16}$ or 32_{16}

and if (Y) ≠ 0 then $i \rightarrow H_{27\text{-}31}$ $H_{0\text{-}26} \rightarrow 0$

$0 \rightarrow Y_i$

$(ILR) + 2 \rightarrow ILR$

or if (Y) = 0 then $(ILR) \rightarrow ILR$

$0 \rightarrow (\text{PS of Program Activity Register})_{APL}$

$0 \rightarrow$ Program Level Lock

If LC = 1, save Process Register 0 only

Attempt level change by auction.

If Y ≥ 40_{16}

and if (Y) ≠ 0 then $i \rightarrow H_{27\text{-}31}$ $0 \rightarrow H_{0\text{-}26}$

$0 \rightarrow Y_i$

$(ILR) + 2 \rightarrow ILR$

or if (Y) = 0 then no operation

70061-590

(1) Address mode 0 is excluded.

(2) Special addresses: process registers and queue registers (privileged status not required).

TQR instruction uses the Hold line of memory for RMW cycles when queue registers are addressed.

Example	Addressing Mode	Action
TQR -18,12	Relative	The effective address is the ILR-18. The contents of the effective address are examined, bit by bit, from left to right. When the first ONE bit is encountered, the bit position is translated to a number and placed in process register 12, bit positions 27 31. The remaining bits of process register 12 are set to ZERO. The bit position that contained the ONE is reset to ZERO and the next instruction in sequence is skipped. If no non-ZERO bits are found, the contents of process register 12 remain unchanged and the next instruction in sequence is executed.

70061-591

Example	Addressing Mode	Action
TQR R'4',11	Direct	The contents of process register 4 are examined, bit by bit, from left to right. When the first ONE bit is encountered, the bit position is translated to a number and placed in process register 11, bit positions 27 31. The remaining bits of process register 11 are set to ZERO. The bit position that contained the ONE is reset to ZERO and the next instruction in sequence is skipped. If no non-ZERO bits are found, the status bit of the active program level in the PAR is reset, the level lock indicator (LLI) in the query register is reset and a program level change is attempted by 'auction' (i.e., the program level that has the highest priority with enable and status bits in the PAR set to ONE will be activated).

70061-592

6-37. Input/Output Instructions

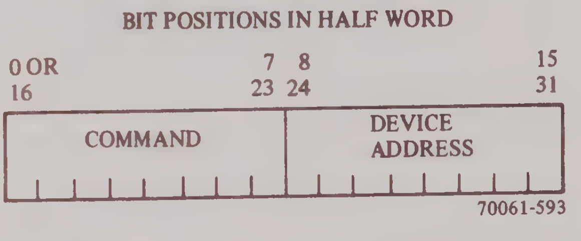
A secondary CPU (without an IOU) executing an Input/Output instruction sets specification violation bit position 5 in the query register.

The following paragraphs describe the input/output instructions.

a. *Device Command (Privileged).* Initially, the Device Time-Out, DT, indicator is reset. The command field of the half-word operand $(Y)_u$ is transmitted to the I/O device specified by the device address field $(Y)_L$. In mode 0, the CA operand is ZERO extended. The DT indicator is set and the instruction is terminated if the addressed device fails to respond to the instruction within 10 microseconds. The instruction H field is not used.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
38	DEV	Y	$(Y)_L$ = Device Address $(Y)_U \rightarrow$ I/O Device	6.0

Operand Format:



70061-593

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
DEV =X'010A	Literal	The most significant eight bits of the literal is the I/O command which is sent to the device address specified by the least significant eight bits of the literal.

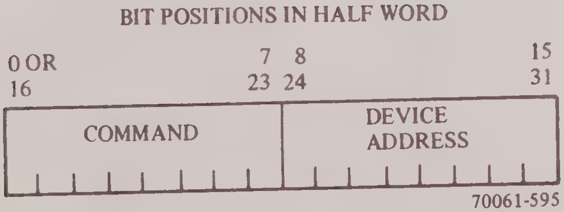
70061-594

b. *Device Command and Exit (Privileged).* Initially, the Device Time-Out, DT, indicator is reset. The command field of the half-word operand $(Y)_u$ is transmitted to the I/O device specified by the device address field $(Y)_L$. In mode 0, the CA operand is ZERO extended. The DT indicator is set and instruction is terminated if the addressed device fails to respond to the instruction within 10 microseconds. The instructions H field is not used. The status bit PS in the program activity register corresponding to the active program level (APL) is reset. The Program Level Lock is reset.

Process register 0 only is saved when the LC indicator is set. If not set, save all process registers. A program level change is attempted at the conclusion of the instruction by auction. Registers are loaded according to the C field in the privilege and level link register of the program level determined by the program level change. Note, that when bit position 9 of the C field is ONE, then access of page control and address registers 4 thru 15 are treated as a memory access violation.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
78	DEX	Y	$(Y)_L$ = Device Address $(Y)_U \rightarrow$ I/O Device $0 \rightarrow$ (PS of Program Activity Register)$_{APL}$ $0 \rightarrow$ Program Level Lock If LC = 1, save Process Register 0 only. Attempt level change by auction	30-10 150

Operand Format:



70061-595

The Program Level Lock is reset. A program level change is initiated by auction. Save only process register 0 if LC = 1; otherwise, all process registers are saved. This program level is terminated and a program level change is attempted.

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
DEX ICON	Direct	The content of the most significant 8 bits of the address ICON is the I/O command which is sent to the device address specified by the content of the least significant 8 bits of address ICON. The status bit of the current active program level is reset in the PAR, the level lock indicator is reset in the query register and a program level change is initiated by 'auction.' (The program level that has the highest priority with enable and status bits in the PAR set to ONE will be activated.)

70061-596

c. *Input to Register (Privileged).* Initially, the input parity error IE and device timeout DT indicators are reset. One to four 8 bit bytes (plus parity) is received from the I/O device specified by the device address field of the half word operand $(Y)_L$ and is loaded into process register H. In mode 0, the CA operand is zero extended. The byte parity is checked. Parity error sets the IE indicator. The received bytes are always stored in H as shown in table 6-6. The DT indicator is set and the instruction is then terminated if the addressed device fails to respond to this instruction within 10 microseconds.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
39	ITR	Y, H	$(Y)_L$ = DEVICE ADDRESS I/O $\rightarrow$ H	6.0

70061-597

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
ITR EQUIP,13	Direct	The content of the least significant 8 bits of address EQUIP contains an I/O device address. From one to four bytes will be received in process register 13 from the device specified by the device address.

70061-598

Table 6-6. Configuration of ITR Data in a Process Register

	0	Bit Positions		31
Process Register Before ITR Data	X X X X	X X X X	X X X X	X X X X
				MSB LSB
Process Register - One Byte Received From Device	0 0 0 0	0 0 0 0	0 0 0 0	Data Byte 1
			MSB LSB	MSB LSB
Process Register Two Bytes Received From Device	0 0 0 0	0 0 0 0	Data Byte 1	Data Byte 2
		MSB LSB	MSB LSB	MSB LSB
Process Register - Three Bytes Received from Device	0 0 0 0	Data Byte 1	Data Byte 2	Data Byte 3
	MSB LSB	MSB LSB	MSB LSB	MSB LSB
Process Register Four Bytes Received from Device	Data Byte 1	Data Byte 2	Data Byte 3	Data Byte 4

MSB Most Significant Bit of Data Byte

LSB Least Significant Bit of Data Byte

70061-18

d. *Output from Register (Privileged).* Initially, the device timeout DT indicator is reset. Four 8 bit bytes (plus generated parity) contained in process register (H) are transmitted to the I/O device specified by the device address field of the half word operand $(Y)_L$. In mode 0, the CA operand is zero extended. The DT indicator is set and the instruction then terminated if the address device fails to respond to this instruction within 10 microseconds.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
79	OFR	Y, H	$(Y)_L$ = DEVICE ADDRESS (H) → I/O	6.0

70061-599

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
OFR $+9,12	Relative	The effective address is the ILR + 9. The least significant 8 bits of the content of the effective address contains an I/O device address. From one to four bytes will be output from process register 12 to the specified device address.

70061-600

6-38. Miscellaneous Instructions

Miscellaneous instructions are described in the following paragraphs.

a. *Conditional Halt (Privileged).* Initially, indicators are not affected. This instruction will halt the computer if one of the following two conditions exist:

If the Computer Test Set (CTS) or System Control Console (SCC) is present and H equals ZERO.

If any one of the four CTS or SCC condition halt switches HSW is ON and its corresponding bit in the H field is a ONE.

If these two conditions do not exist, then a halt does not occur and the next instruction in sequence is executed. The H field of this instruction is used to denote the conditional halt switch or switches which are to be tested. Figure 6-8 illustrates the various values of the H field and the switch(es) each value tests. The word operand (Y) is sent to the CTS or SCC for display. In mode 0, the CA operand is sign extended.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
3A	HLT	Y, H	See Below	4.5

If a CTS or SCC is present:

if $H = 0$, unconditional halt

if $0 < H \leqslant 15$, if one of the 4 CTS or SCC conditional halt switches is on that corresponds to the value in the H field, halt

if a CTS and SCC are not present, no operation.

70061-601

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the word sign position is discarded.

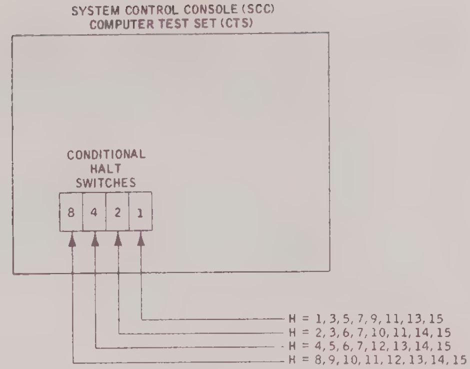

SYSTEM CONTROL CONSOLE (SCC)
COMPUTER TEST SET (CTS)
CONDITIONAL HALT SWITCHES
8
4
2
1
H = 1, 3, 5, 7, 9, 11, 13, 15
H = 2, 3, 6, 7, 10, 11, 14, 15
H = 4, 5, 6, 7, 12, 13, 14, 15
H = 8, 9, 10, 11, 12, 13, 14, 15

Figure 6-8. CTS/SCC Conditional Halt Switches

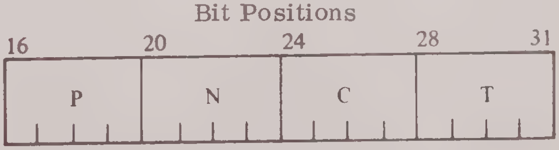
Example	Addressing Mode	Action
HLT DFG,2	Direct	If conditional halt switch 2 is in the on position, the computer halts and displays the contents of address DFG in a bank of lights labeled memory data at the computer test set. If switch 2 is not in the on position, the computer does not halt and the next instruction is executed.

70061-602

b. *Memory Bank Assignment or Test (Privileged).* This instruction uses a 16 bit operand for mode 0 and a 32 bit operand for modes 1, 2 or 3. Mode 0 should be used only when addressing 8K memory banks. Mode 1, 2 or 3 is required for memory banks of any greater size in order to obtain the bank address bits in the proper location of the memory bus.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
7A	MBA	Y	Memory Control	9.1

Mode 0 operand format is as follows:



P:	Present Bank Address for 8K Memories
N:	New Bank Address or Test Control Bits for 8K Memories
C:	Operation Control
T:	Test Control Bits

70061-603

Initially, the memory test, MT, indicator is reset. The half word operand (Y) is transmitted to the memory bank that is specified by the P field. (P field only, shifted left by 2 bit positions.) In mode 0, the CA operand is sign extend.

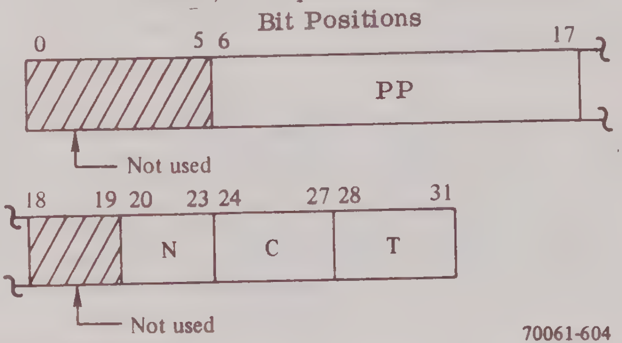
The C field is used to distinguish between memory banks. For C equals 0 to 3, 8K memory banks respond to the P field; if C equals 4 to 7, large memory banks respond to the P field. The assignment of test operation is stipulated by the C field as follows:

C = 0	Memory Test for 8K memory banks.
C = 1	Change present active bank address P to new active bank address N for 8K memory bank.
C = 2	Set present active bank, designated by P, to inactive. N is not used for 8K memory bank.
C = 3	Set present inactive bank, designated by P, to new active bank address N for 8K memory bank.
C = 4 to 7	Same as C = 0 to 3 but for larger than 8K memory bank.

70061-1009

When the memory test operation is selected, the N and T fields determine the test to be executed by the memory bank as shown in table 6-7.

Mode 1, 2 or 3 operand formats are as follows:



70061-604

Table 6-7. Memory Test Options

N				T				
Bit Positions 20	21	22	23	Bit Positions 28	29	30	31	Test *
1	0	0	0	1	0	0	0	Test No. 1
0	1	0	0	1	0	0	0	2
0	0	1	0	1	0	0	0	3
0	0	0	1	1	0	0	0	4
1	0	0	0	0	1	0	0	5
0	1	0	0	0	1	0	0	6
0	0	1	0	0	1	0	0	7
0	0	0	1	0	1	0	0	8
1	0	0	0	0	0	1	0	9
0	1	0	0	0	0	1	0	10
0	0	1	0	0	0	1	0	11
0	0	0	1	0	0	1	0	12
1	0	0	0	0	0	0	1	13
0	1	0	0	0	0	0	1	14
0	0	1	0	0	0	0	1	15
0	0	0	1	0	0	0	1	16

*Depends upon memory type; defined in memory specifications.

70061-19

The 32 bit operand is placed onto the memory bus.

Fields N, C and T operate as previously indicated for mode 0.

Note C field should be set to be 4 – 7.

The PP field allows memories of 8K or greater size to be addressed. The following table defines the bank address bits to be used for various sized memories:

<table>
<tr><th rowspan="3">Memory Bank Size</th><th colspan="13">32 Bit Operand (Modes 1, 2, 3)</th></tr>
<tr><th colspan="13">Bit Positions</th></tr>
<tr><th>6</th><th>7 8 9</th><th>10</th><th>11</th><th>12</th><th>13</th><th>14</th><th>15</th><th>16</th><th>17</th><th></th><th>24</th><th>25</th></tr>
<tr><td>8K</td><td colspan="6">0 ——— 0</td><td colspan="4">B A</td><td></td><td>0</td><td>0</td></tr>
<tr><td>16K</td><td colspan="5">0 ——— 0</td><td colspan="4">B A</td><td>X</td><td></td><td>0</td><td>1</td></tr>
<tr><td>32K</td><td colspan="4">0 ——— 0</td><td colspan="4">B A</td><td>X</td><td>X</td><td></td><td>0</td><td>1</td></tr>
<tr><td>64K</td><td colspan="3">0 ——— 0</td><td colspan="4">B A</td><td>X</td><td>X</td><td>X</td><td></td><td>0</td><td>1</td></tr>
<tr><td>128K</td><td colspan="2">0 ——— 0</td><td colspan="4">B A</td><td>X</td><td>X</td><td>X</td><td>X</td><td></td><td>0</td><td>1</td></tr>
<tr><td colspan="14">BA = Bank Address bits
X Don't care, preferably zero.</td></tr>
</table>

70061-605

In response to this instruction, the selected memory bank will issue the acceptance signal. If a test condition is specified and the test fails, the acceptance signal is not returned. The absence of the acceptance signal will set the MT indicator.

(1) All address modes are permitted.

(2) Special addresses: process registers only.

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

(4) A memory bank in the inactive state only responds to an MBA instruction and if the C field is 3 or 7.

(5) A power on sequence in the memory causes the memory bank to assume its initial bank address and status according to the switch setting. A power off/on sequence with remaining power in the memory bank does not initialize the memory bank.

Example	Addressing Mode	Action
MBA =X'1410'	Literal	The literal specifies a **P** field of 1, an N field of 4, a C field of 1 and a T field of 0. Sets the present active bank address of 1 to a new active bank address 4.

70061-606

c. *Load Call Destination (Semiprivileged).* Initially, the indicators are not affected. The least significant eight bits (8 to 15 or 24 to 31) of the (Y) operand replace the contents in bit position 8 to 15 of the privilege and level link register (C and CPL fields) in memory. Also bits 8 and 9 of the operand are loaded into the Hardware C field. In Mode 0, the CA operand is sign extended. The H field is ignored.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
7D	LOD	Y	$(Y)_L \rightarrow$ (C and CPL)$_{APL}$	7.1

70061-607

(1) All address modes are permitted.

(2) Special addresses: process register only (half).

(3) Mode 0 with indexing: carry out of the half word sign position is discarded.

Example	Addressing Mode	Action
LOD =X'4523'	Literal	Sets the C field in the privilege and level link register of the current active program level to 00 and the CPL field to 35_{10}. (This instruction will use the least significant 8 bits of the literal only.)

70061-608

d. *Level Lock Set (Semiprivileged).* Initially, the indicators are not affected. The program level lock is set. The H, D, A, and W fields are ignored. The M and S fields should be equal to ZERO.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
7B	LLO	See above	1 → program level lock	2.9

70061-609

(1) Address modes do not apply.

(2) Special addresses: not applicable.

Example	Addressing Mode	Action
LLO	None	Set the Program Level Lock.

70061-610

e. *Level Lock Reset.* Initially, the indicators are [illegible] affected. The program level lock is reset. A program level change is attempted only when an I/O device has terminated. The H, D, A, and W fields are ignored. The M and S fields should be ZERO.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
40	LLR	See above	0 → program level lock	2.9

70061-611

(1) Address modes do not apply.

(2) Special addresses: not applicable.

Example	Addressing Mode	Action
LLR	None	Reset the Program Level Lock.

70061-612

f. *Diagnose (Privileged).* Indicators are not affected. The H field controls the diagnose Options 1, 2, and 3. In diagnose Option 1, H = 0, the instruction causes the instruction controller to perform the micro-operations as indicated in figure 6-9. The DIAGNOSE STATUS lights on the front panel display the information as shown in table 6-8. The description to follow applies for the TACFIRE configuration, AN/TSQ-73, AN/TTC-39 and NICS-TARE use LED display. The display interpretation is described in chapter 4 under Diagnose Features, and Front Panel and Maintenance. This diagnose option tests that all ONES and all ZEROS may be transferred to and read from the following CPU registers:

(1) Accumulator (AC) register.

(2) Operand (AY) register.

(3) Process Register 01 (GR).

(4) Memory Data (MD) register.

(5) Instruction Location (CL) register.

(6) Query (PQ) register (bits 00 thru 15).

(7) Indicator (CN) register.

It also tests the exclusive OR function of the CPU by exercising the adder function generator with four different input cases, as shown in figure 6-9.

Table 6-8. Diagnose Lights, Option 1

Diagnose Panel Light	Mnemonic	Function
1	CS00	State Counter
2	CS01	
3	CS02	
4	CS03	
5	CS04	
6	CS05	
7	CS06	
8	CK04	Iteration Counter
9	CK05	Iteration Counter
10	CS07	State Counter
11	ESOT	Automatic Test
12	EEDIGO	Diagnose Option 1

70061-20

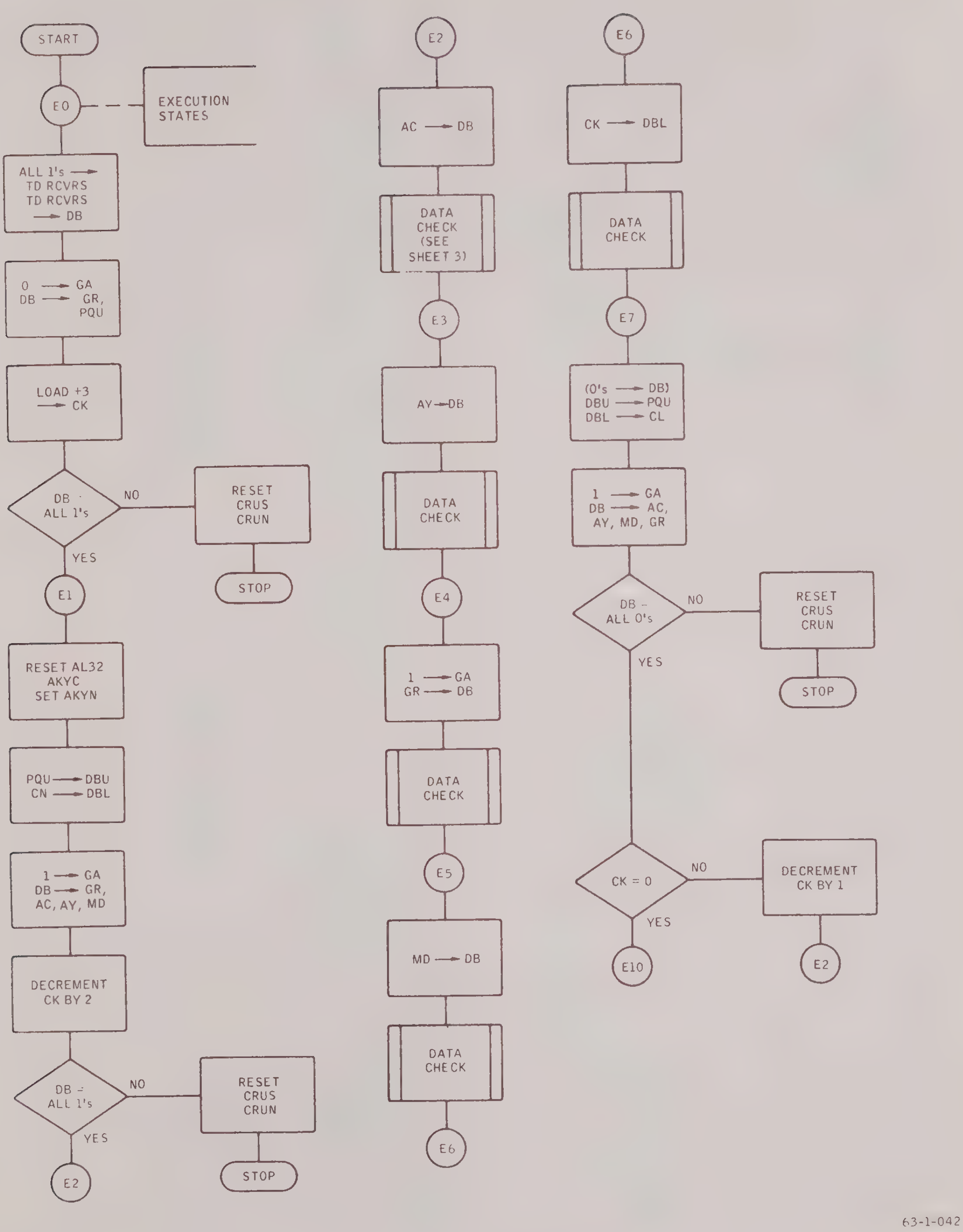

START
E0
EXECUTION STATES
ALL 1's → TD RCVRS
TD RCVRS → DB
0 → GA
DB → GR, PQU
LOAD +3 → CK
DB = ALL 1's
NO
RESET CRUS CRUN
STOP
YES
E1
RESET AL32 AKYC
SET AKYN
PQU → DBU
CN → DBL
1 → GA
DB → GR, AC, AY, MD
DECREMENT CK BY 2
DB = ALL 1's
NO
RESET CRUS CRUN
STOP
YES
E2
E2
AC → DB
DATA CHECK (SEE SHEET 3)
E3
AY → DB
DATA CHECK
E4
1 → GA
GR → DB
DATA CHECK
E5
MD → DB
DATA CHECK
E6
E6
CK → DBL
DATA CHECK
E7
(0's → DB)
DBU → PQU
DBL → CL
1 → GA
DB → AC, AY, MD, GR
DB = ALL 0's
NO
RESET CRUS CRUN
STOP
YES
CK = 0
NO
DECREMENT CK BY 1
E2
YES
E10
63-1-042

Figure 6-9. Diagnose Option 1 Flow Chart (Sheet 1 of 3)

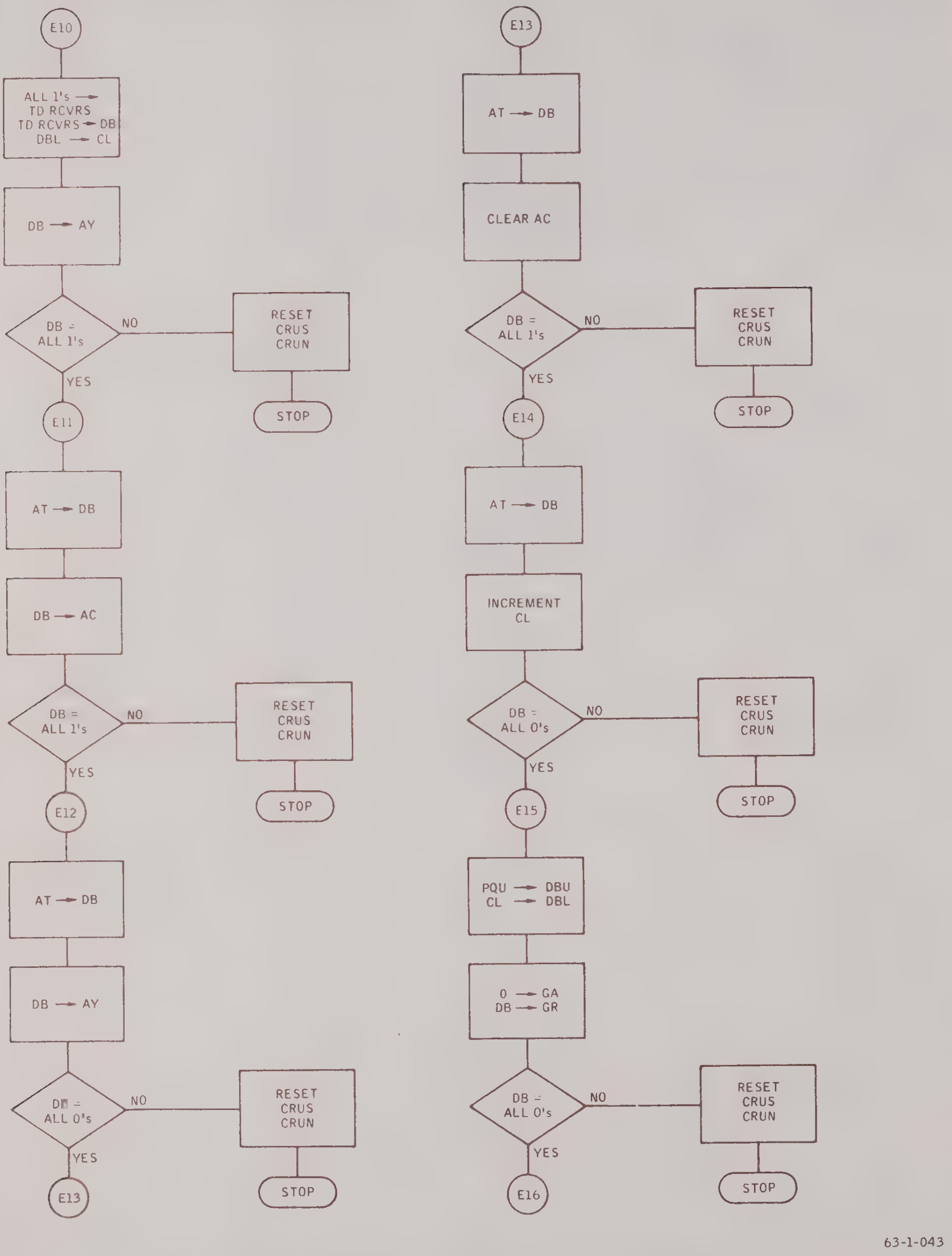
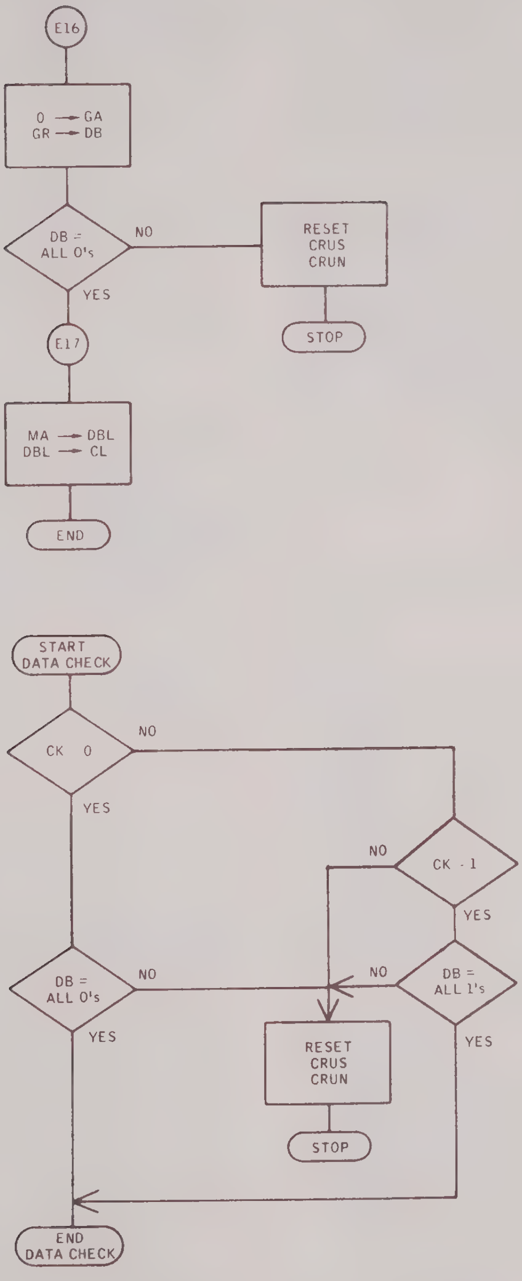

E10
ALL 1's → TD RCVRS
TD RCVRS → DB
DBL → CL
DB → AY
DB = ALL 1's
NO
RESET CRUS CRUN
STOP
YES
E11
AT → DB
DB → AC
DB = ALL 1's
NO
RESET CRUS CRUN
STOP
YES
E12
AT → DB
DB → AY
DB = ALL 0's
NO
RESET CRUS CRUN
STOP
YES
E13
E13
AT → DB
CLEAR AC
DB = ALL 1's
NO
RESET CRUS CRUN
STOP
YES
E14
AT → DB
INCREMENT CL
DB = ALL 0's
NO
RESET CRUS CRUN
STOP
YES
E15
PQU → DBU
CL → DBL
0 → GA
DB → GR
DB = ALL 0's
NO
RESET CRUS CRUN
STOP
YES
E16
63-1-043

Figure 6-9. Diagnose Option 1 Flow Chart (Sheet 2 of 3)


E16
0 → GA
GR → DB
DB = ALL 0's
NO
YES
RESET CRUS CRUN
STOP
E17
MA → DBL
DBL → CL
END
START DATA CHECK
CK 0
NO
YES
CK - 1
NO
YES
DB = ALL 0's
NO
YES
DB = ALL 1's
NO
YES
RESET CRUS CRUN
STOP
END DATA CHECK

70061-185

Figure 6-9. Diagnose Option 1 Flow Chart (Sheet 3 of 3)

AC Value	AY Value	Expected Output
All 0s	All 1s	All 1s
All 1s	All 1s	All 0s
All 1s	All 0s	All 1s
All 0s	All 0s	All 0s

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
3B	DIG	CA, H	See below	10.4

H = 2, 6, A, E Diagnose Option 2; CA and H control diagnose lights

H = 3 Diagnose Option 3; CA = 0 to 3 control diagnose lights

M = 0

S = 0

H = 0 Diagnose Option 1; CA = transfer address; diagnose lights

70061-613

Finally, it tests the ability of the instruction tion register to increment by entering all ONE's o it, incrementing, then examining it for all ZERO's. If an error is detected, then the run flip-flop is reset and the CPU is stopped. The DIAGNOSE STATUS lights will display the error condition on the CPUs diagnose panel. If no error is detected, then the instruction's CA field becomes the address of the next instruction by replacing the contents of the instruction location register. The DIAGNOSE STATUS lights on the CPU's diagnose panel are not turned off following diagnose instruction Option 1; it should be followed by a diagnose Option 2 instruction which can turn off the lights.

g. In diagnose Option 2, H = 2, 6, A, E, the instruction is used to control the 18 DIAGNOSE STATUS lights on the CPU's diagnose panel. The instruction's CA field controls lights 1 to 16 and the H field controls lights 17 and 18. CA bit positions 16 to 31 are associated with lights 1 to 16. A ONE in the corresponding bit position turns the light ON. A ZERO in the corresponding bit position turns the light off.

H = 2 turns light 17 off and light 18 off

H = 6 turns light 17 off and light 18 on

H = A turns light 17 on and light 18 off

H = E turns light 17 on and light 18 on

Then the next instruction in sequence is obtained.

In diagnose Option 3, H = 3, the instruction is used to control the two DIAGNOSE STATUS lights labeled CPU and IOU which are located above the 18 DIAGNOSE STATUS lights on the CPUs diagnose panel. The instruction's CA field controls the lights; only the following values are valid:

CA = 0000 turns light CPU off and light IOU off

CA = 0001 turns light CPU off and light IOU on

CA = 0002 turns light CPU on and light IOU off

CA = 0003 turns light CPU on and light IOU on

70061-1010

Then the next instruction in sequence is obtained. Trap never occurs.

(1) Address modes, and modifications are not permitted. Literal address (without indexing) mode only permitted.

(2) Special addresses: process registers only for Option 1; not applicable for Options 2 and 3.

Example	Addressing Mode	Action
DIG =X'0003',3	Literal without indexing (only allowable mode)	Specifies diagnostic option 3. Turns on the CPU and IOU lights which are located on the CPU diagnose panel.

70061-614

h. *No Operation.* Initially, the indicators are not affected. No operation occurs and the next instruction in normal sequence will be executed.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
00	NOI		No Operation	2.9

70061-615

(1) Address modes do not apply.

(2) Special addresses: not applicable.

Example	Addressing Mode	Action
NOI	None	No operation, the next instruction in sequence is executed.

70061-616

i. *Trap Instructions (Unused Codes).* Initially, the indicators are not affected. The instructions M, H, S, D, A and W fields are ignored. All of the nonimplemented instruction function codes will set the nonimplemented instruction indicator NF, and trap by executing the instruction located in process register 15.

Function Code	Operation Mnemonic	Operand Construction	Symbolic Operation	Time (μsec)
	TRI		See Below	2.9

70061-617

(1) Address modes do not apply.

(2) Special addresses: not applicable.

6-39. Special Addressing Rules.

Special rules apply when an instruction permitted access to all special addresses utilizes either a page control and address register (hex addresses 20 thru 2F) or the query register (hex address 34 or 35) as an operand. These special rules are specified in the following subsections and summarized in table 6-9. Privilege status is required to modify these registers.

a. *Page Control and Address Register.* When a page control and address register is specified as an instruction operand, only the 16-bit register addressed by the least significant 4 bits of the effective operand (Y_{12-15}) is utilized. In full-word instructions which load the operand into a process register, the selected page control and address register is loaded into the least significant half of the selected process register and ZERO-extended. In full-word instructions which store a process register into the operand, the least significant half

Table 6-9. Special Addressing Rules

Instruction	*	Page Control and Address Register		Query Register	
		Page Select	Operation	Operation (W = 0)	Operation (W = 1)
EXF	P	Y_{12-15}	$(H)_{16-31} \rightarrow Y$ $(Y) \rightarrow H_{16-31}$ $0 \rightarrow H_{0-15}$	$(H)_{0-15} \rightarrow Y_{0-15}$ $(Y) \rightarrow H$	$(H)_{0-15} \rightarrow Y_{0-15}$ $(Y) \rightarrow H$
LDF		Y_{12-15}	$(Y) \rightarrow H_{16-31}$ $0 \rightarrow H_{0-15}$	$(Y) \rightarrow H$	$(Y) \rightarrow H$
LDH		Y_{12-15}	$(Y)s \rightarrow H$	$(Y)s \rightarrow H$	$(Y)s \rightarrow H$
MIL	P	Y_{12-15}	$1 \rightarrow Y_{9-15}$	$1 \rightarrow Y_{9-15}$	No Operation
MIU	P	Y_{12-15}	$1 \rightarrow Y_{0-8}$	$1 \rightarrow Y_{0-8}$	No Operation
MZF	P	Y_{12-15}	$0 \rightarrow Y$	$0 \rightarrow Y_{0-15}$	$0 \rightarrow Y_{0-15}$
MZH	P	Y_{12-15}	$0 \rightarrow Y$	$0 \rightarrow Y_{0-15}$	$0 \rightarrow Y_{0-15}$
RBT	P	Y_{12-15}	$0 \rightarrow Y_i$	$0 \rightarrow Y_i$	No Operation
SBT	P	Y_{12-15}	$1 \rightarrow Y_i$	$1 \rightarrow Y_i$	No Operation
SDF	P	Y_{12-15}	$(H)_{16-31} \rightarrow Y$	$(H)_{0-15} \rightarrow Y_{0-15}$	$(H)_{0-15} \rightarrow Y_{0-15}$
SDH	P	Y_{12-15}	$(H)_{16-31} \rightarrow Y^{\#}$	$(H)_{16-31} \rightarrow Y_{0-15}$	No Operation
SMH	P	Y_{12-15}	$(H)_{10-15} \rightarrow Y^{\#}$	$(H)_{0-15} \rightarrow Y_{0-15}$	No Operation
TSO		Y_{12-15}	$ILR + 2 \rightarrow ILR$ if $Y_i = 1$	$ILR + 2 \rightarrow ILR$ if $Y_i = 1$	$ILR + 2 \rightarrow ILR$ if $Y_i = 1$
TSZ		Y_{12-15}	$ILR + 2 \rightarrow ILR$ if $Y_i = 0$	$ILR + 2 \rightarrow ILR$ if $Y_i = 0$	$ILR + 2 \rightarrow ILR$ if $Y_i = 0$

* P, Privilege status required. # Y is active register and image in memory.

70061-2

of the selected process register is stored into the selected page control and address register.

b. *Query Register.* The least significant 16-bits of the query register (level lock indicator, tentative program level and active program level fields) are not modified when utilized as an instruction operand. If a full-word instruction which modifies the operand or a MZH instruction (W = 0 or 1) specifies the query register as an operand, only the most significant 16-bits of the query register will be modified. If a half-word instruction other than a MZH which modifies the operand specifies the query register and has W = 1 (least significant half word selected), no query register modification will occur.

APPENDIX A

LISTS OF AN/GYK-12 MACHINE INSTRUCTIONS

A-1. This appendix contains five separate tables of machine instructions. Figure A-1 provides a cross reference of application and memory type and the appropriate table. Table A-1 lists the instructions by instruction class and also contains the symbolic operation for each instruction.

A-2. Table A-2 lists the machine instructions alphabetically by mnemonic code. Included in this table is a cross reference to the machine instruction description (chapter 6) and to table A-1.

A-3. Table A-3 lists the instructions numerically by function code. Included in the table is a cross reference to the machine instruction description (chapter 6) and to table A-1.

A-4. Table A-4 lists timing by instruction class, indexed by both mnemonic code and numeric function code when used with memories of 2.0 microsecond cycle time.

A-5. Table A-5 lists timing by instruction class, indexed by both mnemonic code and numeric function code. When used with memories of 2.5 microsecond cycle time.

MEMORY TYPE	CYCLE TIME MICROSECOND	APPLICATION	TABLE
8K CORE	2.0	TACFIRE AN/TSQ-73	A-4
MCMU	2.5	TACFIRE AN/TTC-39	A-5
MCMU	2.0	NICS-TARE	A-4

70061-184

Figure A-1. Application Memory Type Cross Reference

Table A-1. AN/GYK-12 Machine Instruction by Instruction Class

INSTRUCTION CLASS: DATA HANDLING

Instruction	Mnemonic	Symbolic Operation	Function Code
Load Full	LDF	$(Y) \rightarrow H$	20
Load Half	LDH	$(Y)_S \rightarrow H$	60
Load Most Half	LMH	$(Y) \rightarrow H_{0-15}$	24
Load From Upper Byte	LDU	$(Y)_U \rightarrow H_{24-31}; 0 \rightarrow H_{0-23}$	21
Load From Lower Byte	LDL	$(Y)_L \rightarrow H_{24-31}; 0 \rightarrow H_{0-23}$	61
Load Absolute Full	LAF	$\lvert (Y) \rvert \rightarrow H$	22
Load Absolute Half	LAH	$\lvert (Y)_S \rvert \rightarrow H$	62
Load Two's Complement Full	LCF	$-(Y) \rightarrow H$	23
Load Two's Complement Half	LCH	$-(Y)_S \rightarrow H$	63
Store Full	SDF	$(H) \rightarrow Y$	26
Store Half	SDH	$(H)_{16-31} \rightarrow Y$, see table 6-9	66
Store Most Half	SMH	$(H)_{0-15} \rightarrow Y$, see table 6-9	64
Store Into Upper Byte	SDU	$(H)_{24-31} \rightarrow Y_U; Y_L$ unchanged	25
Store Into Lower Byte	SDL	$(H)_{24-31} \rightarrow Y_L; Y_U$ unchanged	65
Move All Zeros Full	MZF	$0 \rightarrow Y$	27
Move All Zeros Half	MZH	$0 \rightarrow Y$	67
Move Into Upper Byte	MIU	$I \rightarrow Y_U; Y_L$ unchanged	2D
Move Into Lower Byte	MIL	$I \rightarrow Y_L; Y_U$ unchanged	6D
Exchange Full	EXF	$(H) \rightarrow Y; (Y) \rightarrow H$	2E
Exchange Half	EXH	$(H)_{16-31} \rightarrow Y; (Y)_S \rightarrow H$	6E

70061-22-1

Table A-1. AN/GYK-12 Machine Instruction by Instruction Class (Cont)

INSTRUCTION CLASS: ARITHMETIC

Instruction	Mnemonic	Symbolic Operation	Function Code
Add Full	ADF	$(H) + (Y) \rightarrow H$	08
Add Half	ADH	$(H) + (Y)_S \rightarrow H$	48
Add Logical Full	ALF	$(H) + (Y) \rightarrow H$	0A
Add Logical Half	ALH	$(H) + (Y) \rightarrow H$	4A
Replace Add Full	RAF	$(Y) + (H) \rightarrow Y$	0E
Replace Add Half	RAH	$(Y)_S + (H) \rightarrow Y$	4E
Subtract Full	SBF	$(H) - (Y) \rightarrow H$	09
Subtract Half	SBH	$(H) - (Y)_S \rightarrow H$	49
Subtract Logical Full	SLF	$(H) - (Y) \rightarrow H$	0B
Subtract Logical Half	SLH	$(H) - (Y) \rightarrow H$	4B
Replace Subtract Full	RSF	$(Y) - (H) \rightarrow Y$	0F
Replace Subtract Half	RSH	$(Y)_S - (H) \rightarrow Y$	4F
Multiply Full	MPF	$(H) \times (Y) \rightarrow H_e, H_o$	0C
Multiply Half	MPH	$(H) \times (Y)_S \rightarrow H$	4C
Divide Full	DIF	$(H_e, H_o) \div (Y) \rightarrow H_o, H_e$ or $(H_o)_S \div (Y) \rightarrow H_o, H_e$	0D
Divide Half	DIH	$(H) \div (Y)_S \rightarrow H_o, H_e$	4D
Replace Square Root Full	RQF	$\sqrt{(H)} \rightarrow Y$	1B

70061-22-2

Table A-1. AN/GYK-12 Machine Instruction by Instruction Class (Cont)

INSTRUCTION CLASS: TRANSFER

Instruction	Mnemonic	Symbolic Operation	Function Code
Transfer Unconditionally	XFR	$Z^* \rightarrow ILR$	30
Transfer and Store Link	XLK	$(ILR) \rightarrow H; Z^* \rightarrow ILR$	70
Transfer On Indicators	XIN	If $Ind_i = H_i$, $Z^* \rightarrow ILR$ Otherwise, no operation If $H = 0$, no operation	71
Transfer On Test Switches	XSW	If $TSW_i = H_i$, $Z^* \rightarrow ILR$ Otherwise, no operation If $H = 0$, no operation If $H \neq 0$ and no CTS/SCC is present, no operation	31
Execute	XEX	$Z^* \rightarrow ILR$, Interim	36
Test, Conditionally Decrement by One and Transfer	XDO	If $(H) \neq 0$; $(H) - 1 \rightarrow (H)$ and $Z^* \rightarrow ILR$ If $(H) = 0$, no operation	34
Test, Conditionally Decrement by Two and Transfer	XDT	If $(H) \neq 0$ or 1; $(H) - 2 \rightarrow H$, $Z^* \rightarrow ILR$ If $(H) = 0$ or 1, no operation	74
Test, Conditionally Increment by One and Transfer	XIO	If $(H) \neq 0$; $(H) + 1 \rightarrow (H)$ and $Z^* \rightarrow ILR$ If $(H) = 0$, no operation	35
Test, Conditionally Increment by Two and Transfer	XIT	If $(H) \neq 0$ or 1; $(H) + 2 \rightarrow H$, $Z^* \rightarrow ILR$ If $(H) = 0$ or 1, no operation	75
Transfer if Process Register is Zero	XEF	If $(H) = 0$; $Z^* \rightarrow ILR$ If $(H) \neq 0$, no operation	32
Transfer if Process Register is Not Zero	XUF	If $(H) \neq 0$; $Z^* \rightarrow ILR$ If $(H) = 0$, no operation	72
Transfer if Process Register is Positive	XPF	If $(H) \geq 0$; $Z^* \rightarrow ILR$ If $(H) < 0$, no operation	33
Transfer if Process Register is Negative	XNF	If $(H) < 0$; $Z^* \rightarrow ILR$ If $(H) \geq 0$, no operation	73

INSTRUCTION CLASS: SHIFT

Instruction	Mnemonic	Symbolic Operation	Function Code
Shift Full (or Double)	SHF	(H) shifted $\rightarrow H$ or (H_e, H_o) shifted $\rightarrow H_e, H_o$	1A
Shift Half	SHH	$(H)_{16\text{-}31}$ shifted $\rightarrow H_{16\text{-}31}$	5A

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Table A-1. AN/GYK-12 Machine Instruction by Instruction Class (Cont)

INSTRUCTION CLASS: COMPARE

Instruction	Mnemonic	Symbolic Operation	Function Code
Compare Algebraic Full	CMF	$(Y) : (H) \rightarrow$ Indicator	10
Compare Algebraic Half	CMH	$(Y)_S : (H) \rightarrow$ Indicator	50
Compare Logical Upper Byte	CLU	$(Y)_U : (H)_{24\text{-}31} \rightarrow$ Indicator	11
Compare Logical Lower Byte	CLL	$(Y)_L : (H)_{24\text{-}31} \rightarrow$ Indicator	51
Compare Logical Full	CLF	$(Y) : (H) \rightarrow$ Indicator	12
Compare Logical Half	CLH	$(Y) : (H)_{16\text{-}31} \rightarrow$ Indicator	52
Compare Selective Full	CSF	$(Y) \wedge (R14) : (H) \wedge (R14) \rightarrow$ Indicator	14
Compare Selective Half	CSH	$(Y) \wedge (R14) : (H)_{16\text{-}31} \wedge (R14) \rightarrow$ Indicator	54
Compare Gated Full	CGF	$\lvert (Y) - (H) \rvert : (R14) \rightarrow$ Indicator	13
Compare Gated Half	CGH	$\lvert (Y)_S - (H) \rvert : (R14) \rightarrow$ Indicator	53
Modify and Test Half	MTH	$(Y) + H \rightarrow Y; (Y) : 0 \rightarrow$ indicator	6F

INSTRUCTION CLASS: LOGIC

Instruction	Mnemonic	Symbolic Operation	Function Code
Inclusive OR Full	IOF	$(H) \vee (Y) \rightarrow H$	15
Inclusive OR Half	IOH	$(H)_{16\text{-}31} \vee (Y) \rightarrow H_{16\text{-}31}$	55
Replace Inclusive OR Full	RIF	$(Y) \vee (H) \rightarrow Y$	1D
Replace Inclusive OR Half	RIH	$(Y) \vee (H)_{16\text{-}31} \rightarrow Y$	5D
Exclusive OR Full	EOF	$(H) \veebar (Y) \rightarrow H$	16
Exclusive OR Half	EOH	$(H)_{16\text{-}31} \veebar (Y) \rightarrow H_{16\text{-}31}$	56
Replace Exclusive OR Full	REF	$(Y) \veebar (H) \rightarrow Y$	1E
Replace Exclusive OR Half	REH	$(Y) \veebar (H)_{16\text{-}31} \rightarrow Y$	5E
Logical AND Full	ANF	$(H) \wedge (Y) \rightarrow H$	17
Logical AND Half	ANH	$(H)_{16\text{-}31} \wedge (Y) \rightarrow H_{16\text{-}31}$	57
Replace Logical AND Full	RNF	$(Y) \wedge (H) \rightarrow Y$	1F
Replace Logical AND Half	RNH	$(Y) \wedge (H)_{16\text{-}31} \rightarrow Y$	5F
Selective Substitute Full	SSF	$\lvert (H) \wedge (R14) \rvert \vee \lvert (Y) \wedge (\overline{R14}) \rvert \rightarrow Y$	2F

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Table A-1. AN/GYK-12 Machine Instruction by Instruction Class (Cont)

INSTRUCTION CLASS: BIT

Instruction	Mnemonic	Symbolic Operation	Function Code
Set Bit in Half Word	SBT	$1 \rightarrow Y_i\ (0 \leq i \leq 15)$	1C
Reset Bit in Half Word	RBT	$0 \rightarrow Y_i\ (0 \leq i \leq 15)$	5C
Test Bit in Half Word for Zero, Skip on Match	TSZ	If $(Y)_i = 0$; $(ILR)+2 \rightarrow ILR$ If $(Y)_i \neq 0$, no operation $(0 \leq i \leq 15)$	37
Test Bit in Half Word for One, Skip on Match	TSO	If $(Y)_i = 1$; $(ILR)+2 \rightarrow ILR$ If $(Y)_i \neq 1$; no operation $(0 \leq i \leq 15)$	77
Test and Conditionally Insert/Skip	TSI	$(H)_{16\text{-}31} \vee (Y)_{\text{half word}} \rightarrow (Y)_{\text{half word}}$ If $(Y)_{\text{half word}} = \text{Zero}, (ILR) + 2 \rightarrow (ILR)$ If $(Y)_{\text{half word}} \neq \text{Zero}, (ILR) \rightarrow (ILR)$	76

INSTRUCTION CLASS: FORMAT

Instruction	Mnemonic	Symbolic Operation	Function Code
Format Extract Full	FEF	$[(H)\ \text{shifted}] \wedge (R14) \rightarrow R$	18
Format Extract Half	FEH	$[(H)_{16\text{-}31}\ \text{shifted}] \wedge (R14) \rightarrow R_{16\text{-}31}$	58
Format Insert Full	FIF	$\langle [(H)\ \text{shifted}] \wedge (R14) \rangle \vee \langle (R) \wedge (\overline{R14}) \rangle \rightarrow R$	19
Format Insert Half	FIH	$\langle [(H)_{16\text{-}31}\ \text{shifted}] \wedge (R14) \rangle \vee \langle (R)_{16\text{-}31} \wedge (\overline{R14}) \rangle \rightarrow R_{16\text{-}31}$	59

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Table A-1. AN/GYK-12 Machine Instruction by Instruction Class (Cont)

INSTRUCTION CLASS: PROGRAM LEVEL TRANSFER

Instruction	Mnemonic	Symbolic Operation	Function Code
Call Executive Program Level and Link	TXP	$(Y) \rightarrow (A)_{XPL}$, $APL \rightarrow (LPL)_{XPL}$ $1 \rightarrow (PS)_{XPL}$, $0 \rightarrow (PS)_{APL}$ if $(Y)_0 = 0$, 1 → Program Level Lock, If LC = 1 save Process Register 0 only, Level change to Executive Program Level	3C
Call Program Level and Link	TCP	If $(Y)_1 = 0$ use CPL, If $(Y)_1 = 1$ use level 63, $(Y) \rightarrow (A)_{CPL}$/level 63, $APL \rightarrow (LPL)_{CPL/level\ 63}$, $1 \rightarrow (PS)_{CPL/level\ 63}$, If $(Y)_0 = 0$ then $0 \rightarrow (PS)_{APL}$, If $(Y)_2 = 1$ set i bit in $Queue_{CPL/level\ 63} = (Y)_{3-7}$, 0 → Program Level Lock, If LC = 1 save Process Register 0 only, Attempt level change by auction	7C
Tie Program Level and Link (semiprivileged)	TIE	$(Y) \rightarrow (A)_{APL}$, $APL \rightarrow (LPL)_{CPL}$, If $(Y)_0 = 0$ then $0 \rightarrow (PS)_{APL}$, $1 \rightarrow (PS)_{CPL}$, 1 → Program Level Lock, If LC = 1 save Process Register 0 only, Level change to Tie Program Level	3D
Test and Conditionally Reset/Skip	TQR	1. If $Y = 0$ to $1F_{16}$ or 32_{16} a. $\underline{\text{and if } (Y) \neq 0}$; $i \rightarrow H$, $0 \rightarrow Y_i$ $(ILR) + 2 \rightarrow ILR$ b. $\underline{\text{or if } (Y) = 0}$; $(ILR) \rightarrow ILR$, $0 \rightarrow (PS)_{APL}$, 0 → Program Level Lock, If LC = 1 save Process Register 0 only, Attempt level change by auction 2. If $Y \geq 40_{16}$ a. $\underline{\text{and if } (Y) \neq 0}$; $i \rightarrow H$, $0 \rightarrow Y_i$ $(ILR) + 2 \rightarrow ILR$ b. $\underline{\text{or if } (Y) = 0}$; no operation	5B

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Table A-1. AN/GYK-12 Machine Instruction by Instruction Class (Cont)

INSTRUCTION CLASS: INPUT/OUTPUT

Instruction	Mnemonic	Symbolic Operation	Function Code
Device Command (Privileged)	DEV	$(Y)_L$ = Device address $(Y)_U$ → I/O Device	38
Device Command and Exit (Privileged)	DEX	$(Y)_L$ = Device address $(Y)_U$ → I/O Device 0 → $(PS)_{APL}$, 0 → Program Level Lock, If LC = 1 save Process Register 0 only, Attempt level change by auction	78
Input to Register (Privileged)	ITR	$(Y)_L$ = Device address I/O → H	39
Output from Register (Privileged)	OFR	$(Y)_L$ = Device address (H) → I/O	79

INSTRUCTION CLASS: MISCELLANEOUS

Instruction	Mnemonic	Symbolic Operation	Function Code
Conditional Halt (Privileged)	HLT	If a CTS or SCC is present: If H = 0, unconditional halt If $0 < H \leq 15$, if one of the 4 CTS conditional halt switches is on that corresponds to the value in the H field, halt. If a CTS/SCC is not present, no operation.	3A
Memory Bank Assignment or Test (Privileged)	MBA	Memory Control	7A
Load Call Destination (Semiprivileged)	LOD	$(Y)_L$ → $(C \text{ and } CPL)_{APL}$	7D
Level Lock Set (Semiprivileged)	LLO	1 → Program Level Lock	7B
Level Lock Reset	LLR	0 → Program Level Lock	40
Diagnose (Privileged)	DIG	CPU performs built-in diagnostic functions	3B
No Operation	NOI	No operation	00
Trap Instructions (Unused code)	TRI	Trap by executing instruction in Process Register 15	–

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Table A-2. AN/GYK-12 Machine Instructions – Alphabetic by Mnemonic

Mnemonic	Function Code	Instruction	Page Reference Chapter 6	Page Reference Table A-1
ADF	08	Add Full	6-10	A-3
ADH	48	Add Half	6-10	A-3
ALF	0A	Add Logical Full	6-11	A-3
ALH	4A	Add Logical Half	6-11	A-3
ANF	17	Logical AND Full	6-35	A-5
ANH	57	Logical AND Half	6-35	A-5
CGF	13	Compare Gated Full	6-30	A-5
CGH	53	Compare Gated Half	6-30	A-5
CLF	12	Compare Logical Full	6-28	A-6
CLH	52	Compare Logical Half	6-28	A-5
CLL	51	Compare Logical Lower Byte	6-28	A-5
CLU	11	Compare Logical Upper Byte	6-27	A-5
CMF	10	Compare Algebraic Full	6-27	A-5
CMH	50	Compare Algebraic Half	6-27	A-5
CSF	14	Compare Selective Full	6-29	A-5
CSH	54	Compare Selective Half	6-29	A-5
DEV	38	Device Command (Privileged)	6-46	A-8
DEX	78	Device Command and Exit (Privileged)	6-46	A-8
DIF	0D	Divide Full	6-15	A-3
DIG	3B	Diagnose (Privileged)	6-52	A-8
DIH	4D	Divide Half	6-16	A-3
EOF	16	Exclusive OR Full	6-34	A-5
EOH	56	Exclusive OR Half	6-34	A-5
EXF	2E	Exchange Full	6-9	A-2
EXH	6E	Exchange Half	6-9	A-2
FEF	18	Format Extract Full	6-39	A-6
FEH	58	Format Extract Half	6-40	A-6
FIF	19	Format Insert Full	6-40	A-6
FIH	59	Format Insert Half	6-41	A-6
HLT	3A	Conditioned Halt (Privileged)	6-49	A-8

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Table A-2. AN/GYK-12 Machine Instructions – Alphabetic by Mnemonic (Cont)

Mnemonic	Function Code	Instruction	Page Reference Chapter 6	Page Reference Table A-1
IOF	15	Inclusive OR Full	6-32	A-5
IOH	55	Inclusive OR Half	6-33	A-5
ITR	39	Input To Register (Privileged)	6-47	A-8
LAF	22	Load Absolute Full	6-5	A-2
LAH	62	Load Absolute Half	6-5	A-2
LCF	23	Load 2's Complement Full	6-5	A-2
LCH	63	Load 2's Complement Half	6-6	A-2
LDF	20	Load Full	6-1	A-2
LDH	60	Load Half	6-3	A-2
LDL	61	Load From Lower Byte	6-4	A-2
LDU	21	Load From Upper Byte	6-4	A-2
LLO	7B	Level Lock Set (Semiprivileged)	6-51	A-8
LLR	40	Level Lock Reset	6-52	A-8
LMH	24	Load Most Half	6-4	A-2
LOD	7D	Load Call Destination (Semiprivileged)	6-51	A-8
MBA	7A	Memory Bank Assignment or Test (Privileged)	6-49	A-8
MIL	6D	Move Into Lower Byte	6-9	A-2
MIU	2D	Move Into Upper Byte	6-8	A-2
MPF	0C	Multiply Full	6-14	A-3
MPH	4C	Multiply Half	6-14	A-3
MTH	6F	Modify and Test Half	6-30	A-5
MZF	27	Move All Zeros Full	6-8	A-2
MZH	67	Move All Zeros Half	6-8	A-2
NOI	00	No Operation	6-56	A-8
OFR	79	Output From Register (Privileged)	6-48	A-8
RAF	0E	Replace Add Full	6-11	A-3
RAH	4E	Replace Add Half	6-12	A-3
RBT	5C	Reset Bit in Half Word	6-37	A-6
REF	1E	Replace Exclusive OR Full	6-34	A-5
REH	5E	Replace Exclusive OR Half	6-35	A-5

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Table A-2. AN/GYK-12 Machine Instructions – Alphabetic by Mnemonic (Cont)

Mnemonic	Function Code	Instruction	Page Reference Chapter 6	Page Reference Table A-1
RIF	1D	Replace Inclusive OR Full	6-33	A-5
RIH	5D	Replace Inclusive OR Half	6-33	A-5
RNF	1F	Replace Logical AND Full	6-35	A-5
RNH	5F	Replace Logical AND Half	6-36	A-5
RQF	1B	Replace Square Root Full	6-17	A-3
RSF	0F	Replace Subtract Full	6-13	A-3
RSH	4F	Replace Subtract Half	6-14	A-3
SBF	09	Subtract Full	6-12	A-3
SBH	49	Subtract Half	6-12	A-3
SBT	1C	Set Bit in Half Word	6-37	A-6
SDF	26	Store Full	6-6	A-2
SDH	66	Store Half	6-7	A-2
SDL	65	Store Into Lower Byte	6-7	A-2
SDU	25	Store Into Upper Byte	6-7	A-2
SHF	1A	Shift Full (or Double)	6-24	A-4
SHH	5A	Shift Half	6-26	A-4
SLF	0B	Subtract Logical Full	6-13	A-3
SLH	4B	Subtract Logical Half	6-13	A-3
SMH	64	Store Most Half	6-7	A-2
SSF	2F	Selective Substitute Full	6-36	A-5
TCP	7C	Call Program Level and Link	6-43	A-7
TIE	3D	Tie Program Level and Link (Semiprivileged)	6-44	A-7
TQR	5B	Test and Conditionally Reset/Skip	6-45	A-7
TRI		Trap Instructions (unused codes)	6-57	A-8
TSI	76	Test and Conditionally Insert/Skip	6-38	A-6
TSO	77	Test Bit in Half Word for One, Sip on Match	6-37	A-6
TSZ	37	Test Bit in Half Word for Zero, Skip on Match	6-37	A-6
TXP	3C	Call Executive Program Level and Link	6-42	A-7
XDO	34	Test, Conditionally Decrement by One and Transfer	6-21	A-4

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Table A-2. AN/GYK-12 Machine Instructions – Alphabetic by Mnemonic (Cont)

Mnemonic	Function Code	Instruction	Page Reference Chapter 6	Page Reference Table A-1
XDT	74	Test, Conditionally Decrement by Two and Transfer	6-21	A-4
XEF	32	Transfer If Process Register = 0	6-22	A-4
XEX	36	Execute	6-20	A-4
XFR	30	Transfer Unconditionally	6-18	A-4
XIN	71	Transfer on Indicators	6-19	A-4
XIO	35	Test, Conditionally Increment by One and Transfer	6-21	A-4
XIT	75	Test, Conditionally Increment by Two and Transfer	6-22	A-4
XLK	70	Transfer and Store Link	6-18	A-4
XNF	73	Transfer if Process Register < 0	6-22	A-4
XPF	33	Transfer If Process Register ≥ 0	6-23	A-4
XSW	31	Transfer on Test Switches	6-20	A-4
XUF	72	Transfer if Process Register ≠ 0	6-22	A-4

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Table A-3. AN/GYK-12 Machine Instructions – Numeric by Function Code

Function Code	Mnemonic	Instruction	Page Reference Chapter 6	Page Reference Table A-1
00	NOI	No Operation	6-56	A-8
08	ADF	Add Full	6-10	A-3
09	SBF	Subtract Full	6-12	A-3
0A	ALF	Add Logical Full	6-11	A-3
0B	SLF	Subtract Logical Full	6-13	A-3
0C	MPF	Multiply Full	6-14	A-3
0D	DIF	Divide Full	6-15	A-3
0E	RAF	Replace Add Full	6-11	A-3
0F	RSF	Replace Subtract Full	6-13	A-3
10	CMF	Compare Algebraic Full	6-27	A-5
11	CLU	Compare Logical Upper Byte	6-27	A-5
12	CLF	Compare Logical Full	6-28	A-5
13	CGF	Compare Gated Full	6-30	A-5
14	CSF	Compare Selective Full	6-29	A-5
15	IOF	Inclusive OR Full	6-32	A-5
16	EOF	Exclusive OR Full	6-34	A-5
17	ANF	Logical AND Full	6-35	A-5
18	FEF	Format Extract Full	6-39	A-6
19	FIF	Format Insert Full	6-40	A-6
1A	SHF	Shift Full (or Double)	6-24	A-4
1B	RQF	Replace Square Root Full	6-17	A-3
1C	SBT	Set Bit in Half Word	6-37	A-6
1D	RIF	Replace Inclusive OR Full	6-33	A-5
1E	REF	Replace Exclusive OR Full	6-34	A-5
1F	RNF	Replace Logical AND Full	6-35	A-5
20	LDF	Load Full	6-1	A-2
21	LDU	Load From Upper Byte	6-4	A-2
22	LAF	Load Absolute Full	6-5	A-2
23	LCF	Load 2's Complement Full	6-5	A-2
24	LMH	Load Most Half	6-4	A-2

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Table A-3. AN/GYK-12 Machine Instructions – Numeric by Function Code (Cont)

Function Code	Mnemonic	Instruction	Page Reference Chapter 6	Page Reference Table A-1
25	SDU	Store Into Upper Byte	6-7	A-2
26	SDF	Store Full	6-6	A-2
27	MZF	Move All Zeros Full	6-8	A-2
2D	MIU	Move Into Upper Byte	6-8	A-2
2E	EXF	Exchange Full	6-9	A-2
2F	SSF	Selective Substitute Full	6-36	A-5
30	XFR	Unconditionally Transfer	6-18	A-4
31	XSW	Transfer on Test Switches	6-20	A-4
32	XEF	Transfer if Process Register = 0	6-22	A-4
33	XPF	Transfer if Process Register ≥ 0	6-23	A-4
34	XDO	Test, Conditionally Decrement by One and Transfer	6-21	A-4
35	XIO	Test, Conditionally Increment by One and Transfer	6-21	A-4
36	XEX	Execute	6-20	A-4
37	TSX	Test Bit in Half Word For Zero, Skip on Match	6-37	A-6
38	DEV	Device Command (Privileged)	6-46	A-3
39	ITR	Input To Register (Privileged)	6-47	A-8
3A	HLT	Conditional Halt (Privileged)	6-49	A-8
3B	DIG	Diagnose (Privileged)	6-52	A-8
3C	TXP	Call Executive Program Level and Link	6-42	A-7
3D	TIE	Tie Program Level and Link (Semiprivileged)	6-44	A-7
40	LLR	Level Lock Reset	6-52	A-8
48	ADH	Add Half	6-10	A-3
49	SBH	Subtract Half	6-12	A-3
4A	ALH	Add Logical Half	6-11	A-3
4B	SLH	Subtract Logical Half	6-13	A-3
4C	MPH	Multiply Half	6-14	A-3
4D	DIH	Divide Half	6-16	A-3
4E	RAH	Replace Add Half	6-12	A-3
4F	RSH	Replace Subtract Half	6-14	A-3

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Table A-3. AN/GYK-12 Machine Instructions – Numeric by Function Code (Cont)

Function Code	Mnemonic	Instruction	Page Reference Chapter 6	Page Reference Table A-1
50	CMH	Compare Algebraic Half	6-27	A-5
51	CLL	Compare Logical Lower Byte	6-28	A-5
52	CLH	Compare Logical Half	6-28	A-5
53	CGH	Compare Gated Half	6-30	A-5
54	CSH	Compare Selective Half	6-29	A-5
55	IOH	Inclusive OR Half	6-33	A-5
56	EOH	Exclusive OR Half	6-34	A-5
57	ANH	Logical AND Half	6-35	A-5
58	I I H	Format Extract Half	6-40	A-6
59	FIH	Format Insert Half	6-41	A-6
5A	SHH	Shift Half	6-26	A-4
5B	TQR	Test and Conditionally Reset/Skip	6-45	A-7
5C	RBT	Reset Bit in Half Word	6-37	A-6
5D	RIH	Replace Inclusive OR Half	6-33	A-5
5E	REH	Replace Exclusive OR Half	6-35	A-5
5F	RNF	Replace Logical AND Half	6-36	A-5
60	LDH	Load Half	6-3	A-2
61	LDL	Load From Lower Byte	6-4	A-2
62	LAH	Load Absolute Half	6-5	A-2
63	LCH	Load 2's Complement Half	6-6	A-2
64	SMH	Store Most Half	6-7	A-2
65	SDL	Store Into Lower Byte	6-7	A-2
66	SDH	Store Half	6-7	A-2
67	MZH	Move All Zeros Half	6-8	A-2
6D	MIL	Move Into Lower Byte	6-9	A-2
6E	EXH	Exchange Half	6-9	A-2
6F	MTH	Modify and Test Half	6-30	A-5
70	XLK	Transfer and Store Link	6-18	A-4
71	XIN	Transfer on Indicators	6-19	A-4
72	XUI	Transfer if Process Register $\neq 0$	6-22	A-4
73	XNI	Transfer if Process Register <0	6-22	A-4

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Table A-3. AN/GYK-12 Machine Instructions — Numeric by Function Code (Cont)

Function Code	Mnemonic	Instruction	Page Reference Chapter 6	Page Reference Table A-1
74	XDT	Test, Conditionally Decrement by Two and Transfer	6-21	A-4
75	XIT	Test, Conditionally Increment by Two and Transfer	6-22	A-4
76	TSI	Test and Conditionally Insert/Skip	6-38	A-6
77	TSO	Test Bit in Half Word for One, Skip on Match	6-37	A-6
78	DEX	Device Command (Privileged)	6-46	A-8
79	OFR	Output From Register (Privileged)	6-48	A-8
7A	MBA	Memory Bank Assignment or Test (Privileged)	6-49	A-8
7B	LLO	Level Lock Set (Semiprivileged)	6-51	A-8
7C	TCP	Call Program Level and Link	6-43	A-7
7D	LOD	Load Call Destination (Semiprivileged)	6-51	A-8

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Table A-4. Timing by Classes 2.0 μs Cycle Time

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Data handling	Load register	20	LDF	Load full	4.5	All
		60	LDH	Load half	4.5	All
		24	LMH	Load most half	4.5	All
		21	LDU	Load from upper byte	4.5	All
		61	LDL	Load from lower byte	4.5	All
		22	LAF	Load absolute full	4.5	All
		62	LAH	Load absolute half	4.5	All
		23	LCF	Load 2's complement full	4.5	All
		63	LCH	Load 2's complement half	4.5	All
	Store register	26	SDF	Store full	4.8	No Literal
		66	SDH	Store half	4.8	No Literal
		64	SMH	Store most half	4.8	No Literal
		25	SDU	Store into upper byte	5.0	No Literal
		65	SDL	Store into lower byte	5.0	No Literal
	Move	27	MZF	Move all zeros full	4.8	No Literal
		67	MZH	Move all zeros half	4.8	No Literal
		2D	MIU	Move into upper byte	5.0	Direct W/O Index Only
		6D	MIL	Move into lower byte	5.0	Direct W/O Index Only
	Exchange	2E	EXF	Exchange full		No Literal
		6E	EXH	Exchange half		No Literal
Arithmetic	Fixed-point arithmetic	08	ADF	Add full	4.8	All
		48	ADH	Add half	4.8	All
		0A	ALF	Add logical full	4.8	All
		4A	ALH	Add logical half	4.8	All
		0E	RAF	Replace add full	5.2	No Literal
		4E	RAH	Replace add half	5.2	No Literal
		09	SBF	Subtract full	4.8	All
		49	SBH	Subtract half	4.8	All
		0B	SLF	Subtract logical full	4.8	All
		4B	SLH	Subtract logical half	4.8	All
		0F	RSF	Replace subtract full	5.2	No Literal
		4F	RSH	Replace subtract half	5.2	No Literal
		0C	MPF	Multiply full	16.4	All
		4C	MPH	Multiply half	16.4	All
		0D	DIF	Divide full	18.1	All
		4D	DIH	Divide half	18.1	All
		1B	RQF	Replace square root full	16.6	No Literal

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Table A-4. Timing by Classes 2.0 μs Cycle Time (Cont)

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Transfer (branch)	Control transfer	36	XEX	Execute	4.5	All
		30	XFR	Transfer unconditionally	4.5	All
		70	XLK	Transfer and store link	4.5	All
		31	XSW	Transfer on test switches	4.5	All
		71	XIN	Transfer on indicators	4.5	All
	Index test	34	XDO	Test, conditionally decrement by 1 and transfer	4.8	All
		74	XDT	Test, conditionally decrement by 2 and transfer	4.8	All
		35	XIO	Test, conditionally increment by 1 and transfer	4.8	All
		75	XIT	Test, conditionally increment by 2 and transfer	4.8	All
	Process register test	32	XEF	Transfer if process register = 0	4.5	All
		72	XUF	Transfer if process register ≠ 0	4.5	All
		33	XPF	Transfer if process register ≥ 0	4.5	All
		73	XNF	Transfer if process register < 0	4.5	All
Shift		1A	SHF	Shift full (and double)	4.9 + 0.12K[3]	All
		5A	SHH	Shift half	4.9 + 0.12K	All
Compare		10	CMF	Compare algebraic full	4.7	All
		50	CMH	Compare algebraic half	4.7	All
		11	CLU	Compare logical upper byte	4.8	All
		51	CLL	Compare logical lower byte	4.8	All
		12	CLF	Compare logical full	4.8	All
		52	CLH	Compare logical half	4.8	All
		14	CSF	Compare selective full	5.6	All
		51	CSH	Compare selective half	5.6	All
		13	CGF	Compare gated full	5.4	All
		53	CGH	Compare gated half	5.4	All
		6F	MTH	Modify and test half	4.8	No Literal
		1D	RIF	Replace inclusive OR full	5.1	No Literal
		5D	RIH	Replace inclusive OR half	5.1	No Literal
		16	EOF	Exclusive OR full	4.7	All
		56	EOH	Exclusive OR half	4.7	All
		1E	REF	Replace exclusive OR full	5.1	No Literal
		5E	REH	Replace exclusive OR half	5.1	No Literal
		17	ANF	Logical AND full	4.7	All
		57	ANH	Logical AND half	4.7	All

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Table A-4. Timing by Classes 2.0 μs Cycle Time (Cont)

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Logic		15	IOF	Inclusive OR full	4.7	All
		55	IOH	Inclusive OR half	4.7	All
		1D	RIF	Replace inclusive OR full	5.1	No Literal
		5D	RIH	Replace inclusive OR half	5.1	No Literal
		16	EOF	Exclusive OR full	4.7	All
		56	EOH	Exclusive OR half	4.7	All
		1E	REF	Replace exclusive OR full	5.1	No Literal
		5E	REH	Replace exclusive OR half	5.1	No Literal
		17	ANF	Logical AND full	4.7	All
		57	ANH	Logical AND half	4.7	All
		1F	RNF	Replace logical AND full	5.1	No Literal
		5F	RNH	Replace logical AND half	5.1	No Literal
		2F	SSF	Selective substitute full	4.7	No Literal
Bit		1C	SBT	Set bit in half word	5.0	No Literal
		5C	RBT	Reset bit in half word	5.0	No Literal
		37	TSZ	Test bit in half word for zero, skip on match	4.8	No Literal
		77	TSO	Test bit in half word for one, skip on match	4.8	No Literal
		76	TSI	Test and conditionally insert/skip	5.3	No Literal
Format		18	FEF	Format extract full	5.3 + 0.12K[3]	All
		58	FEH	Format extract half	5.3 + 0.12K	All
		19	FIF	Format insert full	5.9 + 0.12K	All
		59	FIH	Format insert half	5.9 + 0.12K	All
Program level transfer		3C	TXP	Call executive program level and link	30 to 150[4]	All
		7C	TCP	Call program level and link	30 to 150[4]	All
		3D	TIE	Tie program level and link (semiprivileged)	30 to 150[4]	All
		5B	TQR	Test and conditionally reset skip	6 to 150[4]	No Literal
Input/Output		38	DEV	Device command (privileged)	6.0	All
		78	DEX	Device command, and exit (privileged)	30 to 150[4]	All
		39	ITR	Input to register (privileged)	6.0	All
		79	OFR	Output from register (privileged)	6.0	All

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Table A-4. Timing by Classes 2.0 μs Cycle Time (Cont)

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Miscellaneous		3A	HLT	Conditional halt (privileged)	4.5	All
		7A	MBA	Memory bank assignment or test (privileged)	10.0	No Literal
		7D	LOD	Load call destination (semiprivileged)	7.1	All
		7B	LLO	Level lock set (semiprivileged)	2.9	None
		40	LLR	Level lock reset	2.9	None
		3B	DIG	Diagnose (privileged)	10.4	Literal W/O Index Only
		00	NOI	No operation	2.9	None
			TRI	Trap instructions (unused codes)	2.9	None

[1] The direct address mode without indexing and without instruction-operand memory access overlap are assumed in the instruction execution times (8K memories).

[2] Time increase or decrease dependent on address mode. Execution times measured with respect to a memory having a 2.0 microsecond cycle time and zero length cable delay. Add 10 nanoseconds per foot of cable length.

K = bit positions shifted.

[4] Includes total time from instruction initiate until next instruction may be executed; since these instructions involve program level changes, minimum and maximum time including program level changing, are shown.

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Table A-5. Timing by Classes, 2.5 μs Cycle Time

Instructions						
Class	Subclass	Function Code	Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Data Handling	Load Register	20	LDF	Load full	5.3	All
		60	LDH	Load half	5.3	All
		24	LMH	Load most half	5.3	All
		21	LDU	Load from upper byte	5.3	All
		61	LDL	Load from lower byte	5.3	All
		22	LAF	Load absolute full	5.5	All
		62	LAH	Load absolute half	5.5	All
		23	LCF	Load 2's complement full	5.5	All
		63	LCH	Load 2's complement half	5.5	All
	Store Register	26	SDF	Store full	6.0	No Literal
		66	SDH	Store half	6.0	No Literal
		64	SMH	Store most half	6.0	No Literal
		25	SDU	Store into upper byte	6.2	No Literal
		65	SDL	Store into lower byte	6.2	No Literal
	Move	27	MZF	Move all zeros full	6.0	No Literal
		67	MZH	Move all zeros half	6.0	No Literal
		2D	MIU	Move into upper byte	6.2	Direct W/O Index Only
		6D	MIL	Move into lower byte	6.2	Direct W/O Index Only
	Exchange	2E	EXF	Exchange full	6.5	No Literal
		6E	EXH	Exchange half	6.5	No Literal
Arithmetic	Fixed-point Arithmetic	08	ADF	Add full	5.5	All
		48	ADH	Add half	5.5	All
		0A	ALF	Add logical full	5.5	All
		4A	ALH	Add logical half	5.5	All
		0E	RAF	Replace add full	6.2	No Literal
		4E	RAH	Replace add half	6.2	No Literal
		09	SBF	Subtract full	5.5	All
		49	SBH	Subtract half	5.5	All
		0B	SLF	Subtract logical full	5.5	All
		4B	SLH	Subtract logical half	5.5	All
		0F	RSF	Replace subtract full	6.2	No Literal
		4F	RSH	Replace subtract half	6.2	No Literal
		0C	MPF	Multiply full	17.2	All
		4C	MPH	Multiply half	17.2	All
		0D	DIF	Divide full	18.8	All
		4D	DIH	Divide half	18.8	All
		1B	RQF	Replace square root full	17.6	No Literal

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Table A-5. *Timing by Classes, 2.5 μs Cycle Time (Cont)*

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Transfer (Branch)	Control Transfer	36	XEX	Execute	5.3	All
		30	XFR	Transfer unconditionally	5.3	All
		70	XLK	Transfer and store link	5.3	All
		31	XSW	Transfer on test switches	5.3	All
		71	XIN	Transfer on indicators	5.3	All
	Index test	34	XDO	Test, conditionally decrement by 1 and transfer	5.5	All
		74	XDT	Test, conditionally decrement by 2 and transfer	5.5	All
		35	XIO	Test, conditionally increment by 1 and transfer	5.5	All
		75	XIT	Test, conditionally increment by 2 and transfer	5.5	All
	Process Register Test	32	XEF	Transfer if process register $= 0$	5.3	All
		72	XUF	Transfer if process register $\neq 0$	5.3	All
		33	XPF	Transfer if process register ≥ 0	5.3	All
		73	XNF	Transfer if process register < 0	5.3	All
Shift		1A	SHF	Shift full (and double)	5.5 + 0.12K[3]	All
		5A	SHH	Shift half	5.5 + 0.12K	All
Compare		10	CMF	Compare algebraic full	5.4	All
		50	CMH	Compare algebraic half	5.4	All
		11	CLU	Compare logical upper byte	5.6	All
		51	CLL	Compare logical lower byte	5.6	All
		12	CLF	Compare logical full	5.4	All
		52	CLH	Compare logical half	5.4	All
		14	CSF	Compare selective full	6.4	All
		51	CSH	Compare selective half	6.4	All
		13	CGF	Compare gated full	6.2	All
		53	CGH	Compare gated half	6.2	All
		6F	MTH	Modify and test half	6.4	No Literal

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Table A-5. Timing by Classes, 2.5 μs Cycle Time (Cont)

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Logic		15	IOF	Inclusive OR full	5.4	All
		55	IOH	Inclusive OR half	5.4	All
		1D	RIF	Replace inclusive OR full	6.0	No Literal
		5D	RIH	Replace inclusive OR half	6.0	No Literal
		16	EOF	Exclusive OR full	5.4	All
		56	EOH	Exclusive OR half	5.4	All
		1E	REF	Replace exclusive OR full	6.0	No Literal
		5E	REH	Replace exclusive OR half	6.0	No Literal
		17	ANF	Logical AND full	5.4	All
		57	ANH	Logical AND half	5.4	All
		11	RNF	Replace logical AND full	6.0	No Literal
		51	RNH	Replace logical AND half	6.0	No Literal
		2F	SSF	Selective substitute full	6.6	No Literal
Bit		1C	SBT	Set bit in half word	6.2	No Literal
		5C	RBT	Reset bit in half word	6.2	No Literal
		37	TSZ	Test bit in half word for ZERO, skip on match	5.5	No Literal
		77	TSO	Test bit in half word for ONE, skip on match	5.5	No Literal
		76	TSI	Test and conditionally insert/skip	5.8	No Literal
Format		18	FEF	Format extract full	6.0 + 0.12K[3]	All
		58	FEH	Format extract half	6.0 + 0.12K	All
		19	FIF	Format insert full	6.5 + 0.12K	All
		59	FIH	Format insert half	6.5 + 0.12K	All
Program Level Transfer		3C	TXP	Call executive program level and link	29 to 128[4]	All
		7C	TCP	Call program level and link	33 to 146[4]	All
		3D	TIE	Tie program level and link (semiprivileged)	29 to 128[4]	All
		5B	TQR	Test and conditionally reset/skip	7 to 136[4]	No Literal
Input/Output		38	DEV	Device command (privileged)	7.0	All
		78	DEX	Device command, and exit (privileged)	29 to 136[4]	All
		39	ITR	Input to register (privileged)	7.0	All
		79	OFR	Output from register (privileged)	7.0	All

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Table A-5. Timing by Classes, 2.5 μs Cycle Time (Cont)

Instructions			Mnemonic	Name	Nominal Execution Time[1] (Microseconds)	Execution Time Variables Applicable[2]
Class	Subclass	Function Code				
Miscellaneous		3A	HLT	Conditional halt (privileged)	5.3	All
		7A	MBA	Memory bank assignment or test (privileged)	8.0	No Literal
		7D	LOD	Load call destination (semiprivileged)	7.1	All
		7B	LLO	Level lock set (semiprivileged)	3.0	None
		40	LLR	Level lock reset	3.0	None
		3B	DIG	Diagnose (privileged)	10.8	Literal W/O Index Only
		00	NOI	No operation instruction	3.0	None
			TRI	Trap instructions (unused codes)	3.0	None

---

[1] The direct address mode without indexing and without instruction-operand memory access overlap are assumed in the instruction execution times.

[2] Time increase or decrease dependent on address modes. Execution times measured with respect to a memory having a 2.5 μsec cycle time and zero length cable delay. Add 10 nanoseconds per foot of cable length.

[3] K = bit positions shifted.

[4] Includes total time from instruction initiate until next instruction may be executed; since these instructions involve program level changes, minimum and maximum times including program level changing, are shown.

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APPENDIX B

PERIPHERAL INTERFACE

Section I. INTRODUCTION

B1-1. Scope

This appendix to the AN/GYK-12 COMPUTER PRINCIPLES OF OPERATION MANUAL, contains software-oriented information regarding various computer peripheral devices and their interfaces. Capabilities of these peripheral devices are defined, and peripheral details are given on how the peripheral devices are controlled.

The subject peripheral devices are all related to the AN/GYK-12(V) computer. This document also provides some programming examples; however, it must be pointed out that most of the applications used are unique, and establishment of hard and fast rules for their usage is not feasible.

B1-2. Purpose

The information presented in this document is intended to aid in the design and implementation of programs required for the control and use of the peripheral devices described.

B1-3. Organization of Document

General information of programming input/output (I/O) operations is provided in Section B2. Each of the remaining sections cover information of a specific peripheral device. The data within each of these sections is organized into the following subsections:

a. *General.* Briefly describes the purpose of the peripheral device.

b. *Capabilities.* Concisely states the capabilities and limitations imposed by the hardware on the subject peripheral device.

c. *References.* Supplies a list of documents that may be used for additional information of the peripheral device.

d. *Computer Interface.* Describes the peripheral-to-computer interface and subdevice interfaces, where applicable.

e. *Command and Control Word(s).* Defines the type of control words used, their format, and (when applicable) provides a description of control-words content and usage.

f. *Status Word(s).* Defines the status word format, and (when applicable) provides a description of status-word content and usage.

g. *Interrupts.* Defines the purpose(s) of the device-caused interrupt; states whether an attendant Interrupt Status Word Byte is generated; and if this word byte is generated, gives its format, content, and usage.

h. *Data Structure.* Defines the data structures that may be used when transferring data to, or from, the peripheral device.

i. *Special Considerations.* Provides brief statements on considerations to be made when writing a program that employs a peripheral device.

Section II. INPUT/OUTPUT

This section provides general information on computer input/output (I/O) and includes some data on I/O programming conventions. The I/O referred to in this document serves three distinct purposes:

a. Control of peripheral devices.

b. Status determination of peripheral devices.

c. Transfer of data to and from peripheral devices.

All of the peripheral devices covered in this document use some form of control and provide an indication of their status, but not all of these peripheral devices require data transfers.

B2-1. I/O Instructions

Control of peripheral devices and status information from a peripheral device is accomplished via the following computer I/O instructions:

a. *Device Command (DEV).* The DEV causes a predefined 8-bit code to be transferred to the specified peripheral device, commanding it to perform a given function.

NOTE

> Not all peripheral devices respond to Device commands.

b. *Device Command and Exit (DEX).* The DEX operates the same as DEV, with the addition that current program level is terminated.

c. *Input to Register (ITR).* The ITR causes a peripheral device to be interrogated for a status message, or it can be used to provide a programmed input of a discrete word of one to four 8-bit bytes. The register to receive this word is defined as part of the ITR instruction format.

NOTE

> Where a peripheral device has more than one status word, selection of the desired word may be via an Output from Register (OFR): or status words may be returned sequentially (i.e., one for each ITR executed) with the actual word determination left to the software.

d. *Output from Register (OFR).* The OFR causes a programmed output of a discrete word of four 8-bit bytes to a peripheral device. The register containing the word to be output is defined as part of the OFR instruction format.

NOTE

> Although four bytes are always transferred, not all peripheral devices use all of the bytes.

B2-2. Peripheral Device Input/Output Operations

The individual peripheral device requirements govern accomplishment of control by the DEV and OFR instructions. Status information from a peripheral device is requested via the ITR instruction, or status information is brought to the computer's attention by the peripheral device's initiating an Interrupt.

Once an I/O instruction is executed, actual data transfers proceed automatically in accordance with the mode specified in the current keyword for the given device. Programming conventions normally have used a DEV instruction to initiate block input and output data transfers, while ITR and OFR commands normally are used for individual word transfers in keeping with their defined purposes. The automatic transfer of data is terminated once the block length field in the keyword is counted down to zero. Subsequently, the previously defined termination word is used to determine what actions are to be taken as a result of the I/O completion.

The importance of proper keyword and termination word handling/setup prior to initiating any I/O on a given channel cannot be overemphasized. Because the block-length field of the keyword is decremented as a result of automatic I/O operations, the keyword for a given channel must be reinitialized prior to any I/O olving data transfers on that channel. Also, certain fields in the termination word are affected by the I/O operations, thereby requiring the termination word be reinitialized before any data transfers.

A further consideration for keywords and termination words is that subsequent to data transfer I/O operations, the keyword mode should be set to inactive to prevent any inadvertent transfer of data. This also should be done or verified in the case where only control functions are to be accomplished (i.e., rewind).

Figure B2-1 illustrates an automatic input or output operation, showing the flow of the software and hardware functions.

B2-3. Computer Interface

That portion of the computer I/O operation which is fixed by hardware covers all actual byte transfers and attendant timing and control signals. Figure B2-2 illustrates the various sequences associated with command code and data transfers. It should be noted that Device control and Device command are two distinctly separate terms. The Device control byte contents are fixed by the hardware, whereas the Device command byte contents are controlled by the software: figure B2-3 defines the allowable Device control byte contents.

Operation of the instructions used consist of the following:

a. *Device Command (DEV) Operation.* The DEV command consists of an address selection phase, employing the command line, and a device control phase with information lines 0 and 3 activated, followed by a single data byte of which is used for control purposes. The peripheral device acknowledges receipt of this command sequence by activating the indicator line after receiving the data byte.

b. *Output from Register (OFR) Operation.* The OFR command consists of an address selection phase employing the command line, and a device control phase with information lines 0 and 4 activated followed by four data bytes. The peripheral device acknowledges receipt of this command by activating the indicator line after receiving any of the data bytes.

c. *Input to Register (ITR) Operation.* The ITR sequence consists of an address selection phase employing the command line, followed by a device control phase employing information lines 0 and 5, followed by one or four data bytes generated by the peripheral device. The peripheral device activates the indicator line when sending the last data byte.

d. *End of Block (EOB) Operation.* The EOB sequence consists of an address selection phase employing the command line followed by a device control phase employing information lines 0 and 6. The peripheral device may send a request any time after recognizing the control information.

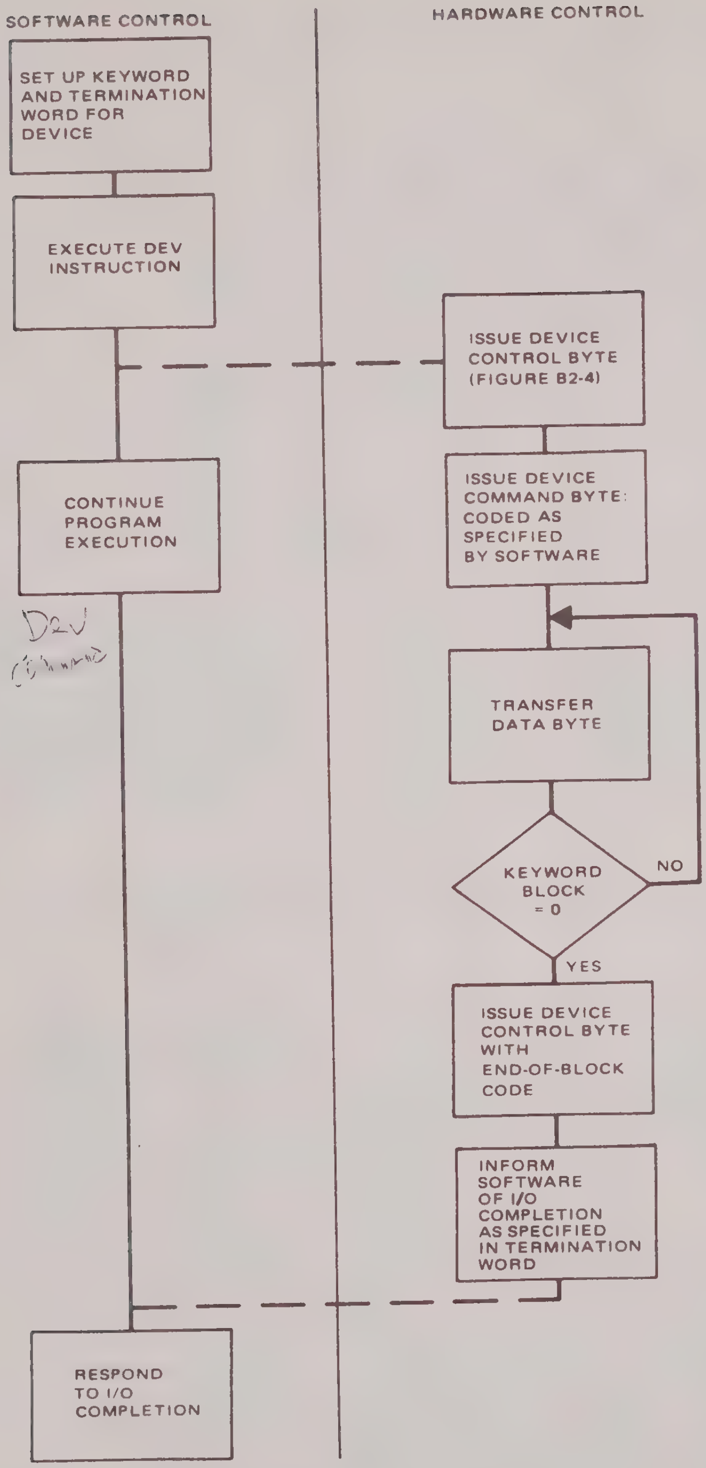
SOFTWARE CONTROL
HARDWARE CONTROL
SET UP KEYWORD AND TERMINATION WORD FOR DEVICE
EXECUTE DEV INSTRUCTION
ISSUE DEVICE CONTROL BYTE (FIGURE B2-4)
CONTINUE PROGRAM EXECUTION
ISSUE DEVICE COMMAND BYTE: CODED AS SPECIFIED BY SOFTWARE
TRANSFER DATA BYTE
KEYWORD BLOCK = 0
NO
YES
ISSUE DEVICE CONTROL BYTE WITH END-OF-BLOCK CODE
INFORM SOFTWARE OF I/O COMPLETION AS SPECIFIED IN TERMINATION WORD
RESPOND TO I/O COMPLETION
D2V
[illegible]

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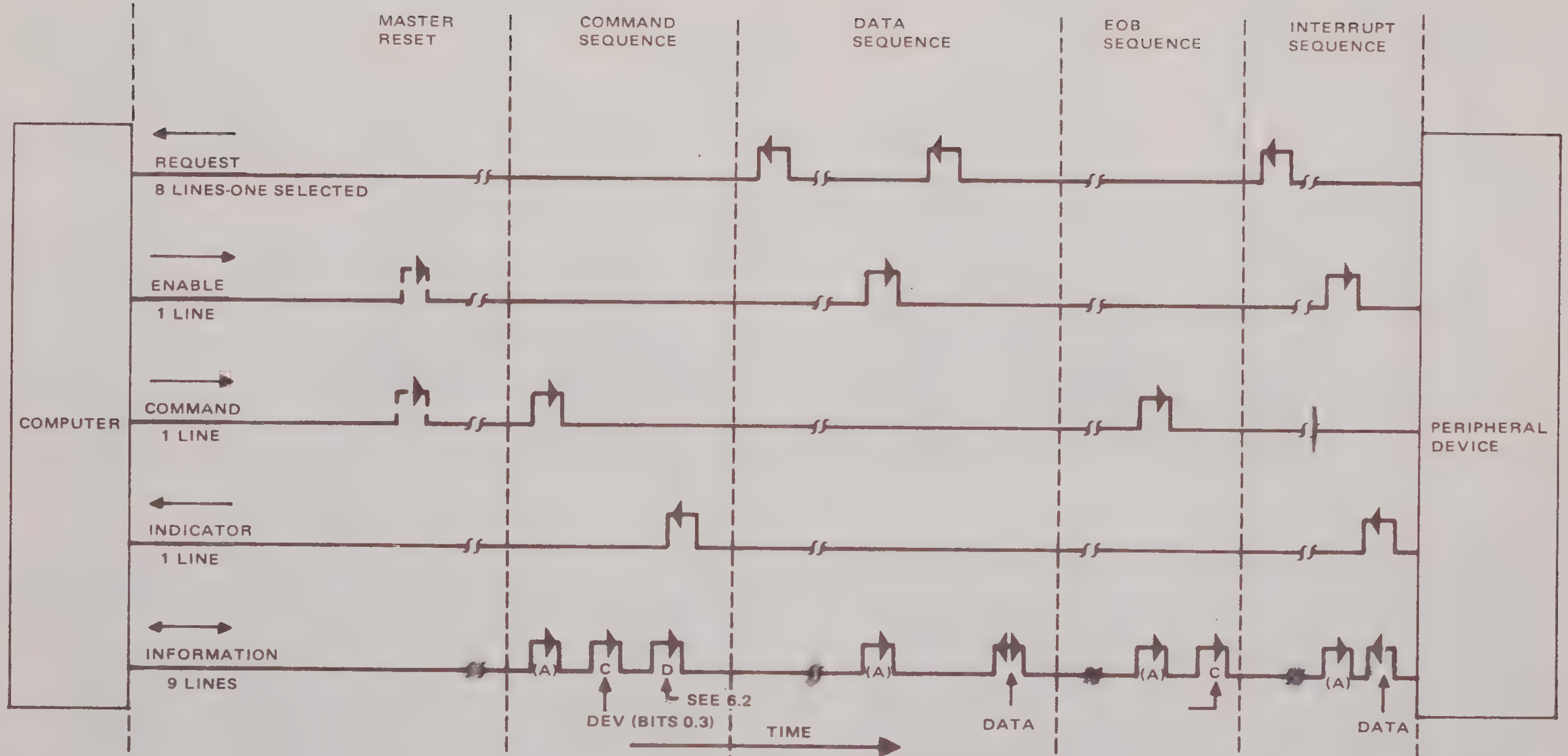
Figure B2-1. Automatic Input/Output Sequence


MASTER RESET
COMMAND SEQUENCE
DATA SEQUENCE
EOB SEQUENCE
INTERRUPT SEQUENCE
COMPUTER
REQUEST
8 LINES-ONE SELECTED
ENABLE
1 LINE
COMMAND
1 LINE
INDICATOR
1 LINE
INFORMATION
9 LINES
PERIPHERAL DEVICE
(A)
C
D
SEE 6.2
DEV (BITS 0.3)
DATA
(A)
C
(A)
DATA
TIME

NOTE: ARROWS INDICATE DIRECTION OF SIGNAL FLOW

1. TIMING BETWEEN PULSES FOR ALL TIMING DIAGRAMS IS IN ACCORDANCE WITH COMPUTER I/O SPEC 587650-620

(A) = DEVICE ADDRESS
C = DEVICE CONTROL BYTE (TABLE 2-1)
I = INTERRUPT DATA BYTE
D = DEVICE COMMAND BYTE

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Figure B2-2. Computer, Peripheral Interface

Bits Present During Control Phase	Function
0 and 3	DEVICE COMMAND (DEV)
0 and 4	OUTPUT FROM REGISTER (OFR)
0 and 5	INPUT TO REGISTER (ITR)
0 and 6	END OF BLOCK (EOB)
0 and 7	DEVICE STOP

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Figure B2-3. Device Control Format on Information Lines

e. *Stop Operation.* This operational sequence consists of an address selection phase employing the command line followed by a device control phase employing information lines 0 and 7. The sequence is generated by the computer when an illegal or erroneous condition occurs. It may occur after a request for service for an automatic input or output operation. When the peripheral device detects this operation, it reverts to its standby state.

B2-4. Peripheral Device Summary Data

The following figures provide summary information on the various peripheral devices covered in this document. Device control applicability, figure B2-4, defines which peripheral devices respond to which control commands. Device interrupt generation, figure B2-5, shows which peripheral devices generate interrupts under which conditions, and which peripheral devices provide interrupt data bytes.

Section III. ARTILLERY CONTROL CONSOLE

B3-1. ACC General

The artillery control console (ACC) is the primary command interface for the TACFIRE System. The ACC contains three semi-autonomous subdevices (figure B3-1).

a. The Compose Edit (C/E) subdevice provides for the generation of control messages, using a keyboard and a CRT display unit.

b. The Receive Display (RD) subdevice provides for displaying of various received messages on a CRT display unit.

c. The Switch Assembly (SA) subdevice provides for actual control of data transfers to the computer and general overall ACC switch action control.

Of the three subdevices, actions of the SA can be considered as being of highest priority because it has most of the action switches and provides overall data distribution.

B3-2. ACC Capabilities

The displays used are approximately 3 by 8.5 inches in size with a capability of displaying 7 rows of 72 characters each. The displayable character set and/or the set the keyboard is capable of generating as shown in figure B3-2. Storage for the display data is internal to the display units, thereby eliminating any need for computer refresh cycles.

B3-3. ACC Reference

ACC Development Specification, EL-CP-00041105

B3-4. ACC-to-Computer Interface

Data transfers between the computer and ACC are performed on an automatic input/output and interrupt basis (figure B3-3). Communication is via a mixture of bytes and 32-bit words with actual data transfers being accomplished on an 8-bit byte basis. Each ACC subdevice (SA, C/ED and RD) (figure B3-4) is assigned an individual but adjacent, channel, resulting in each having a separate request line; however, all other lines are common.

DEV Control Byte	ACC	ARMM	DDT	DPM	ELP	ETD	CSIN	SIU
DEVICE COMMAND	X	X	X	-	X	-	X	X
OFR	X	X	-	X	X	X	-	-
ITR	X	X	X	X	X	X	X	X
EOB	X	X	X	X	X	X	X	X
DEVICE STOP	X	X	X	-	X	X	X	X

X = Device Responds to Function

- = Device does not recognize function

ACC = Artillery Control Console
ARMM = Auxiliary Removable Media Memory
DDT = Digital Data Terminal
DPM = Digital Plotter Map
ELP = Electronic Line Printer
ETD = Electronic Tactical Display
CSIN = Communications Security Interface Network
SIU = System Interface Unit

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Figure B2-4. Peripheral Device Control Applicability Table

Interrupt Generation Function	ACC			ARMM	DDT		DPM	ELP	ETD	CSIN		SIU
	SA	CE	RD		XMT	RCV				INPUT	OUT	
EOB		IB	IB	IB			IB	IB				IB
FAULT COND	I			IB				IB		I		IB
OPERATOR	I						IB		I(2)			
OTHER						I(1)						

I = Interrupt generated

IB = Interrupt generated and interrupt data byte provided

(1) Signifies end of received message

(2) Light pen

60113-5

Figure B2-5. Device Interrupt Generation

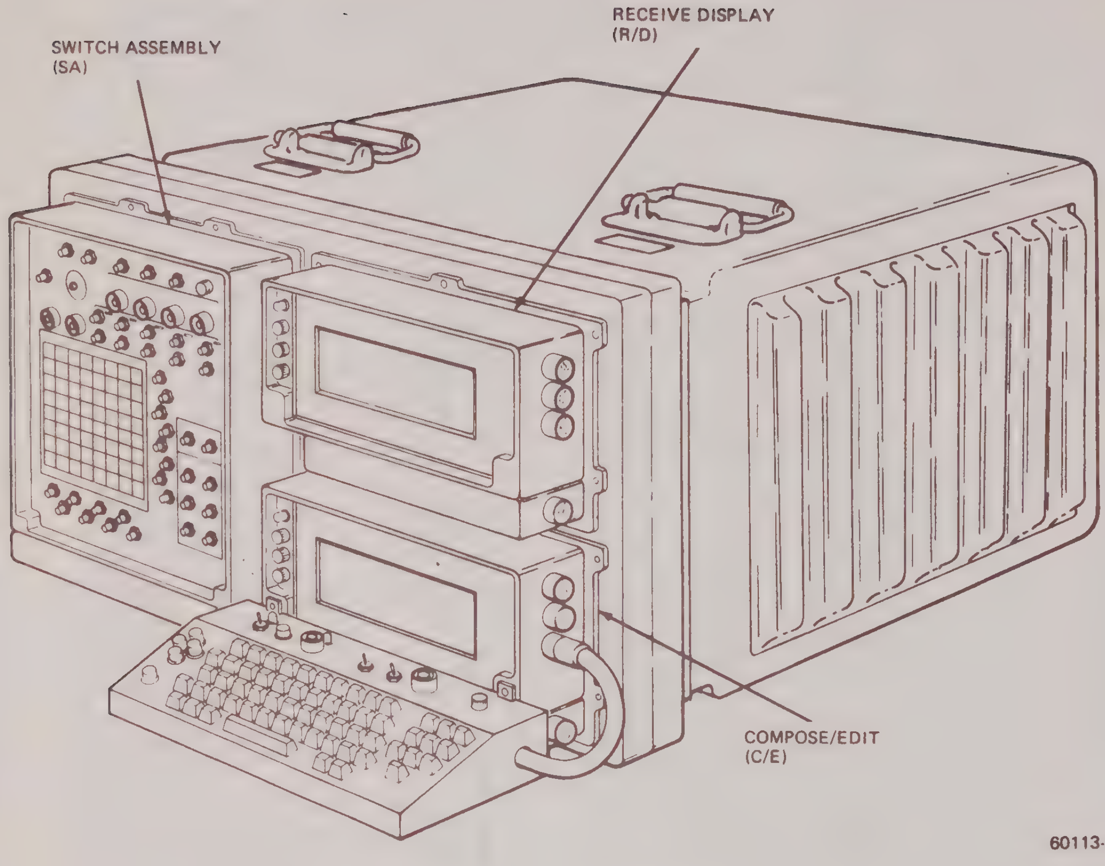

Figure B3-1. ACC Subdevices

B3-5. ACC Command and Control Word(s)

The three subdevices that make up the ACC are for the most part controlled individually, with the SA being the central distributor. There are two types of control used for the ACC: (1) an OFR word for the SA and, (2) device command bytes for the C/E and RD.

a. *SA OFR Word.* This word is used to control the various indicators on the SA and, via the setting and resetting of the Q state FF, to control the active or quiescent state of the ACC itself (figure B3-5).

b. *Device Command Bytes.* These bytes are basically the same format that is used to control the C/E and RD (figures B3-6, B3-7, and B3-8).

B3-6. ACC Status Word(s)

The status of the ACC subdevices are sent to the mputer in the form of individual ITR words when an ITR command for a subdevice is issued by the computer (ITR instruction for desired subdevices is executed). The format and purpose of the ITR words are defined in the following paragraphs and figures:

a. *SA ITR Word.* This word provides the status of the various SA action switches, C/E and R/D fault indicators, and the activity state of the ACC itself (figure B3-9).

b. *C/E ITR Word.* This word provides the status of the SA matrix row and column switches, C/E channel status, C/E and RD fault indication, and the activity state of the ACC itself (figure B3-10).

c. *RD ITR Word.* This word provides the status of the SA Message Address Switches, C/E and RD fault indicators, and the activity state of the ACC itself (figure B3-11).

Column →				0	1	2	3	4	5	6	7	Row
b7				0	0	0	0	1	1	1	1	↓
b6				0	0	1	1	0	0	1	1	
b5				0	1	0	1	0	1	0	1	
b4	b3	b2	b1									
0	0	0	0	NUL	DLE	SP	0	@	P	@	P	0
0	0	0	1	SOH	DC1	!	1	A	Q	A	Q	1
0	0	1	0	STX	DC2	"	2	B	R	B	R	2
0	0	1	1	ETX	DC3	#	3	C	S	C	S	3
0	1	0	0	EOT[1]	DC4	$	4	D	T	D	T	4
0	1	0	1	ENQ	NAK[1]	%	5	E	U	E	U	5
0	1	1	0	ACK[1]	SYN	&	6	F	V	F	V	6
0	1	1	1	BEL	ETB	' (apos)	7	G	W	G	W	7
1	0	0	0	BS	CAN	(	8	H	X	H	X	8
1	0	0	1	HT	EM	)	9	I	Y	I	Y	9
1	0	1	0	LF	SS	*	:	J	Z	J	Z	10
1	0	1	1	VT	ESC	+	;	K	[	K	'	11
1	1	0	0	FF	FS	,	<	L	\	L	\	12
1	1	0	1	CR	GS	-	=	M	]	M	]	13
1	1	1	0	SO	RS	.	>	N	∧	N	∧	14
1	1	1	1	SI	US	/	?	O	-	O	-	15

[1] Columns 0 and 1 are nondisplay control codes except for

EOT	(⅃),	end of transmission
ACK	(⋈),	acknowledge
NAK	(⊗),	negative acknowledge

[2] The noncoded diamond (◇) symbol is displayed to indicate receipt of an erroneous character.

[3] Example of code:

P	b7	b6	b5	b4	b3	b2	b1
1	0	1	0	0	1	0	0

= $

MSB LSB

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Figure B3-2. Alphanumeric Display Character Set (66 Symbol Subset)

Subdevice	OFR Word	DEV Comm Byte	ITR Word	ASCII Data Byte	Interrupt Request	Interrupt Byte
SA	0	-	I	-	I	-
C/E	-	0	I	I/0	I	I
RD	-	0	I	I/0	I	I

NOTE: I = Computer Input from Subdevice
0 = Computer Output to Subdevice

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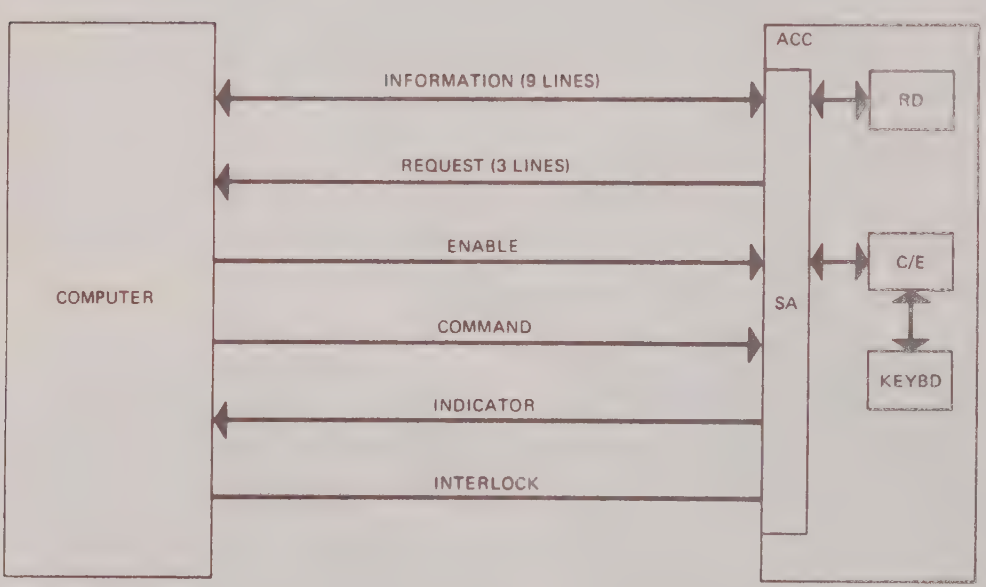
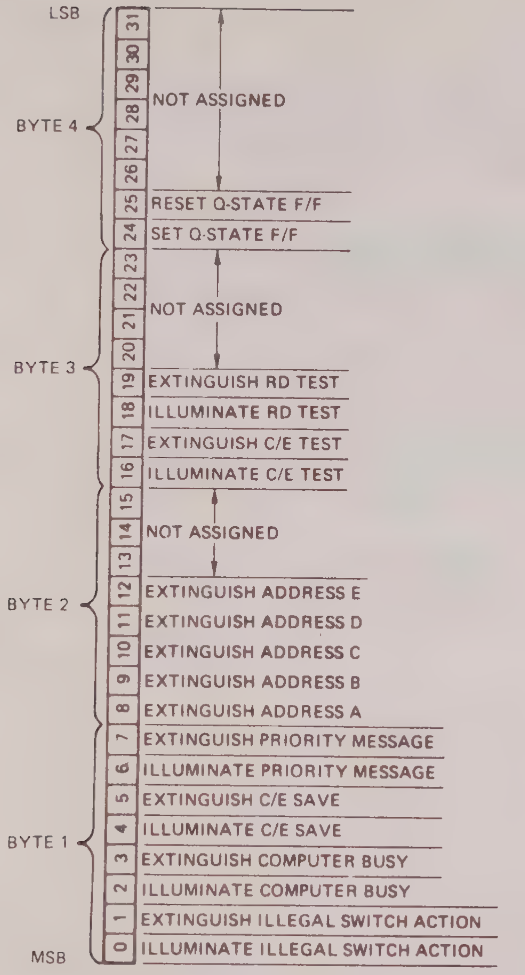
Figure B3-3. ACC Subdevice-to-Computer Interface Data


ACC
INFORMATION (9 LINES)
RD
REQUEST (3 LINES)
ENABLE
C/E
COMPUTER
SA
COMMAND
KEYBD
INDICATOR
INTERLOCK

NOTE:
THREE REQUEST LINES ARE UTILIZED BY THE ACC

60113-9

Figure B3-4. ACC Computer Interface


LSB
31
30
29
28
27
26
NOT ASSIGNED
BYTE 4
25
RESET Q-STATE F/F
24
SET Q-STATE F/F
23
22
21
20
NOT ASSIGNED
BYTE 3
19
EXTINGUISH RD TEST
18
ILLUMINATE RD TEST
17
EXTINGUISH C/E TEST
16
ILLUMINATE C/E TEST
15
14
13
NOT ASSIGNED
BYTE 2
12
EXTINGUISH ADDRESS E
11
EXTINGUISH ADDRESS D
10
EXTINGUISH ADDRESS C
9
EXTINGUISH ADDRESS B
8
EXTINGUISH ADDRESS A
7
EXTINGUISH PRIORITY MESSAGE
6
ILLUMINATE PRIORITY MESSAGE
5
EXTINGUISH C/E SAVE
4
ILLUMINATE C/E SAVE
BYTE 1
3
EXTINGUISH COMPUTER BUSY
2
ILLUMINATE COMPUTER BUSY
1
EXTINGUISH ILLEGAL SWITCH ACTION
0
ILLUMINATE ILLEGAL SWITCH ACTION
MSB

60113-10

Figure B3-5. SA OFR Word Format

B3-7. ACC Interrupts

Since each subdevice of the ACC has its own channel assigned, each is capable of generating an individual interrupt.

C/E and RD interrupts are similar in that both cause an interrupt data byte to be put on the data lines as part of the interrupt sequence. C/E and RD interrupt sequences are generated as follows:

a. To terminate an Automatic Input exchange on the C/E channel.

b. In response to an EOB from the computer to terminate an Automatic exchange.

In both cases an interrupt data byte is put on the data lines (figure B3-12).

The SA interrupt is unique in that it does not cause the interrupt data byte to be generated as part of the interrupt sequence. SA interrupts are generated as follows:

a. If a C/E or RD fault is detected.

b. If the C/E or RD does not accept an ASCII character from the SA.

c. If a switch corresponding to a bit in the SA ITR word is depressed.

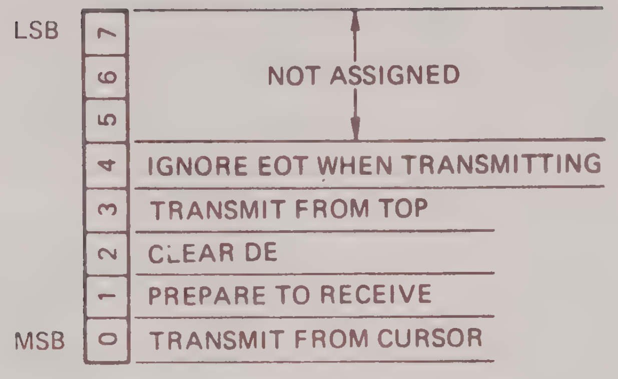
Once the SA interrupt is received, further processing is required to determine the required response by requesting the SA ITR word.

B3-8. ACC Data Structures

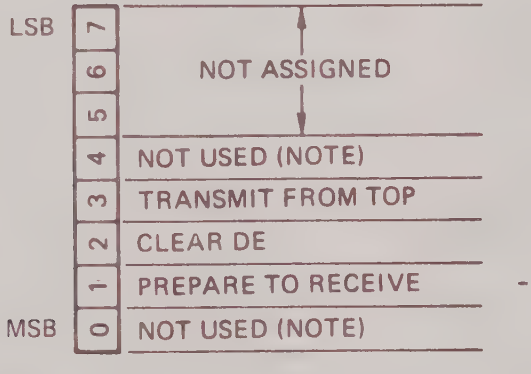
No specific data structure is required to output to the RD and/or the C/E. The data to be transferred are ASCII characters so the data buffers can contain only this type of data; no control information is included in the buffer. Figure B3-13 illustrates the ASCII data byte as it is transferred across the interface. The SA has no data transfers for its own use and therefore does not require any data buffer.

B3-9. ACC Special Considerations

The Q state FF controls the active/quiescent state of the ACC as a unit. Once this FF is reset no communications can take place other than the SA OFR word which can set it. During the quiescent state none of the ACC subdevices will respond to ITRs or Device commands.


LSB
7
6
5
NOT ASSIGNED
4
IGNORE EOT WHEN TRANSMITTING
3
TRANSMIT FROM TOP
2
CLEAR DE
1
PREPARE TO RECEIVE
MSB
0
TRANSMIT FROM CURSOR

a. C/E DEV BYTE


LSB
7
6
5
NOT ASSIGNED
4
NOT USED (NOTE)
3
TRANSMIT FROM TOP
2
CLEAR DE
1
PREPARE TO RECEIVE
MSB
0
NOT USED (NOTE)

b. RD DEV BYTE

NOTE: SINCE THE RD DE SHALL TRANSMIT ONLY FOR TEST PURPOSES, THESE TWO COMMANDS ARE NOT NECESSARY. THE CPU SHALL ALWAYS CAUSE THE WHOLE DE DISPLAY TO BE TRANSMITTED AND EOTs SHALL NOT CAUSE TERMINATION.

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Figure B3-6. C/E and RD Device Command Bytes

Bit	Description
0	Transmit from cursor. Causes the C/E channel to engage in an Automatic Input data transfer with the computer. The C/E begins sending characters to the computer starting at the current cursor location and terminates when EOT is encountered.
1	Prepare to Receive. Causes the C/E channel to engage in an Automatic Output data transfer with the computer. The C/E begins receiving characters from computer starting at the current cursor location.
2	Clear DE. Causes the C/E to be cleared and the cursor to be positioned to the upper left character position.
3	Transmit from Top. Causes the C/E channel to engage in an Automatic Input data transfer with the computer. The C/E begins sending characters to the computer starting from the upper left character position.
4	Ignore EOT when Transmitting. Causes the C/E channel not to terminate an Automatic Input data transfer to the computer when an EOT is encountered.
5 through 7	Not assigned.

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Figure B3-7. C/E Device Command Byte Content and Usage

Bit	Description
0	Not used.
1	Prepare to Receive. Causes the RD channel to engage in an Automatic Output data transfer with the computer. The RD begins receiving characters from computer starting at the current cursor location.
2	Clear DE. Causes the RD to be cleared and the cursor to be positioned to the upper left character position.
3	Transmit from Top. Causes the RD channel to engage in an Automatic Input data transfer with the computer. The RD begins sending characters to the computer starting from the upper left character position.
4 through 7	Not assigned.

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Figure B3-8. RD Device Command Byte Content and Usage

	Bit	Function
LSB	31	NOT ASSIGNED
	30	NOT ASSIGNED
	29	Q-STATE F/F
BYTE 4	28	RD NONTRANSFER
	27	C/E NONTRANSFER
	26	SPARE
	25	RD DE FAULT
	24	C/E DE FAULT
	23	NOT ASSIGNED
	22	SPARE COMMAND SWITCH
	21	CANCEL CHECK FIRING
BYTE 3	20	FINAL PROTECTIVE FIRE
	19	CHECK FIRING
	18	NOT ASSIGNED
	17	RD TEST
	16	C/E TEST
	15	ILLEGAL SWITCH ACTION
	14	TRANSFER TO EDIT
	13	DELETE
BYTE 2	12	RD COMPUTER ACTION
	11	RD TRANSMIT
	10	PAGE
	9	CYCLE MESSAGES
	8	PRIORITY MESSAGE
	7	PRINT
	6	C/E TRANSMIT
	5	FORMAT SELECT
BYTE 1	4	FORMAT COMMAND
	3	RESTORE
	2	SAVE
	1	REPLACE
MSB	0	C/E COMPUTER ACTION

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Figure B3-9. SA ITR Word Format

	Bit	Function
LSB	31	NOT ASSIGNED
	30	NOT ASSIGNED
	29	Q-STATE F/F
BYTE 4	28	RD NONTRANSFER
	27	C/E NONTRANSFER
	26	SPARE
	25	RD DE FAULT
	24	C/E DE FAULT
	23	MATRIX COLUMN 8
	22	MATRIX COLUMN 7
	21	MATRIX COLUMN 6
BYTE 3	20	MATRIX COLUMN 5
	19	MATRIX COLUMN 4
	18	MATRIX COLUMN 3
	17	MATRIX COLUMN 2
	16	MATRIX COLUMN 1
	15	MATRIX ROW H
	14	MATRIX ROW G
	13	MATRIX ROW F
BYTE 2	12	MATRIX ROW E
	11	MATRIX ROW D
	10	MATRIX ROW C
	9	MATRIX ROW B
	8	MATRIX ROW A
	7	NOT ASSIGNED
	6	
	5	
BYTE 1	4	
	3	
	2	
	1	
MSB	0	CHANNEL BUSY

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Figure B3-10. C/E ITR Word Format

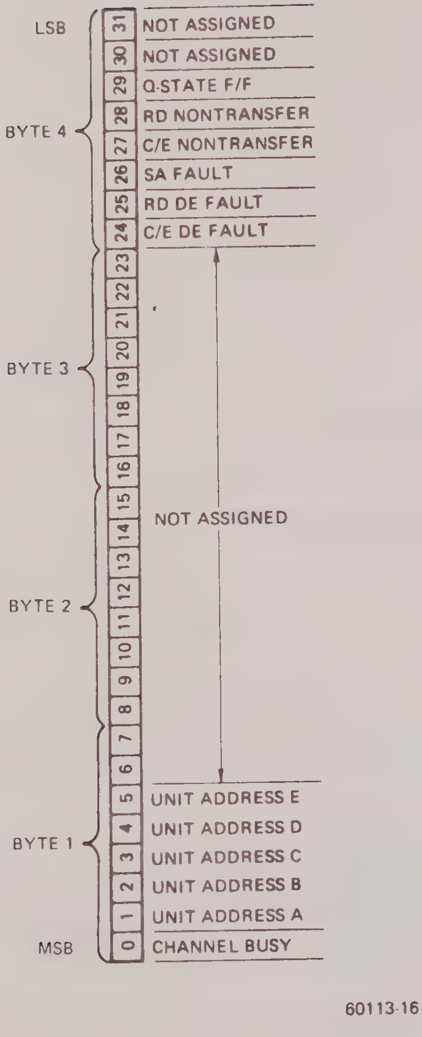
LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31 NOT ASSIGNED
30 NOT ASSIGNED
29 Q-STATE F/F
28 RD NONTRANSFER
27 C/E NONTRANSFER
26 SA FAULT
25 RD DE FAULT
24 C/E DE FAULT
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
NOT ASSIGNED
5 UNIT ADDRESS E
4 UNIT ADDRESS D
3 UNIT ADDRESS C
2 UNIT ADDRESS B
1 UNIT ADDRESS A
0 CHANNEL BUSY
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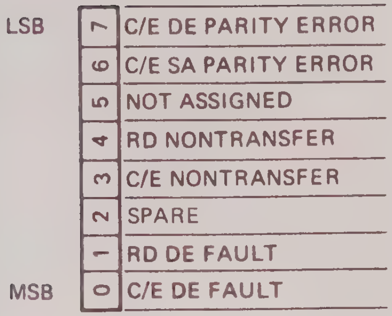
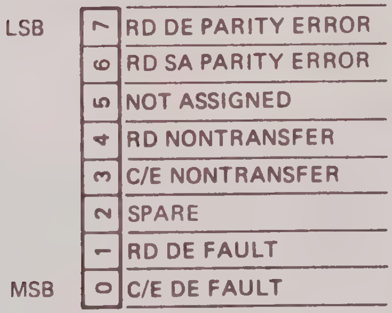
Figure B3-11. RD ITR Word Format


LSB
MSB
7 C/E DE PARITY ERROR
6 C/E SA PARITY ERROR
5 NOT ASSIGNED
4 RD NONTRANSFER
3 C/E NONTRANSFER
2 SPARE
1 RD DE FAULT
0 C/E DE FAULT

a. C/E INTERRUPT BYTE


LSB
MSB
7 RD DE PARITY ERROR
6 RD SA PARITY ERROR
5 NOT ASSIGNED
4 RD NONTRANSFER
3 C/E NONTRANSFER
2 SPARE
1 RD DE FAULT
0 C/E DE FAULT

b. RD INTERRUPT BYTE

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Figure B3-12. C/E and RD Interrupt Bytes

LSB	7	ASCII b1
	6	ASCII b2
	5	ASCII b3
	4	ASCII b4
	3	ASCII b5
	2	ASCII b6
	1	ASCII b7
MSB	0	PARITY (ODD)

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Figure B3-13. C/E and RD ASCII Data Byte

Section IV. AUXILIARY REMOVABLE MEDIA MEMORY

B4-1. ARMM General

The auxiliary removable media memory (ARMM) is used for loading of programs into computer memory and the recording and retrieval of data under computer control. The ARMM utilizes a sealed removable tape transport cartridge for the actual recording and tape handling functions (figure B4-1). A single ARMM in a transit case is a memory loading unit (MLU). Two ARMM's in a transmit case makes up a removable media memory unit (RMMU).

B4-2. ARMM Capabilities

The actual limits for data storage and tape handling operations are set by the removable cartridge which contains the magnetic tape, transport hardware, and read/write heads.

B4-3. ARMM References

ARMM Development Specification, EL-CP-00041103

ARMM Technical Manual, TM11-7440-245-35

B4-4. ARMM Computer Interface

Data transfers between the computer and ARMM are performed on an automatic input/output and interrupt basis. Communication is via bytes and words with actual data transfers being accomplished on an 8-bit byte basis. The interface lines are illustrated in figure B4-2.

B4-5. ARMM Command and Control Word(s)

Control of the ARMM by the computer is accomplished, using two types of command formats, defined as follows:

a. *ARMM OFR Word.* Only the most significant byte of this word is used by the ARMM for a loop test. The byte is sent back to the computer by the ARMM with no modification. The initial transfer results from the execution of an OFR instruction for the ARMM by the computer. Figure B4-3 illustrates the OFR word format.

b. *Device Command Byte.* The commands issued for READ, WRITE, etc. fall into this category. Figure B4-4 illustrates the Device Command format and figure B4-5 defines the various codes.

B4-6. ARMM Status Word(s)

Device status information is returned to the computer from the ARMM in the form of an ITR word composed of one 8-bit byte. The execution of an ITR instruction by the computer causes the byte illustrated in figure B4-6 to be transferred. Figure B4-7 defines the ITR word contents.

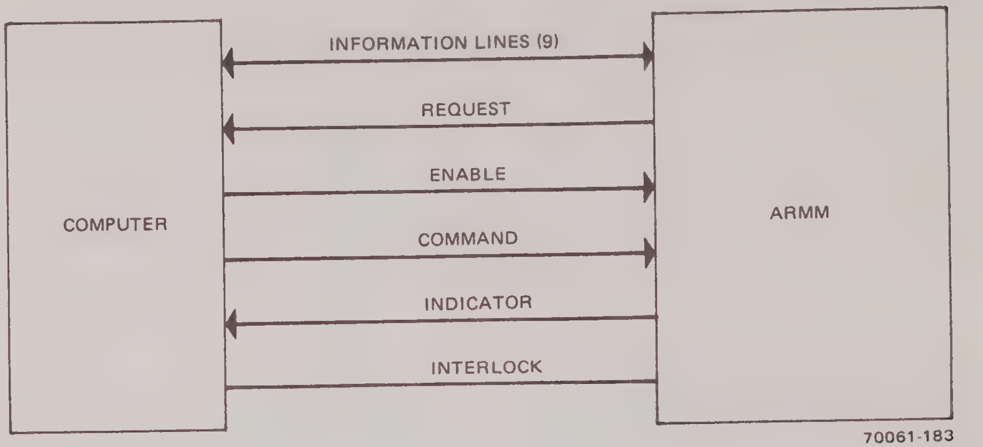
COMPUTER
INFORMATION LINES (9)
REQUEST
ENABLE
COMMAND
INDICATOR
INTERLOCK
ARMM
70061-183

Figure B4-2. ARMM Computer Interface

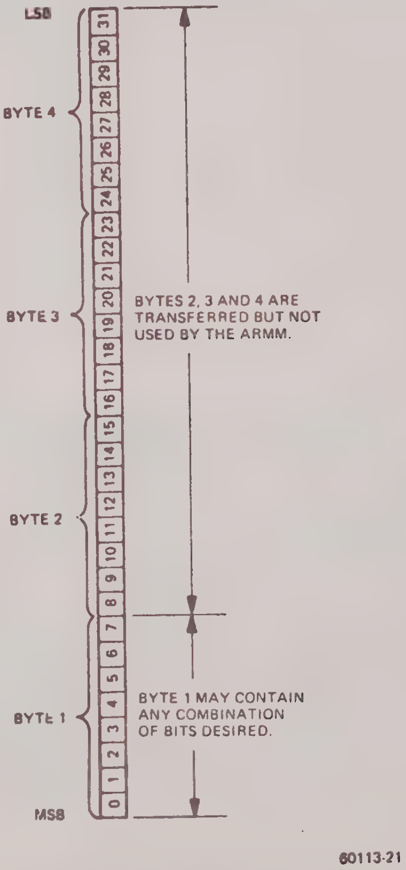
LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
BYTES 2, 3 AND 4 ARE TRANSFERRED BUT NOT USED BY THE ARMM.
BYTE 1 MAY CONTAIN ANY COMBINATION OF BITS DESIRED.
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Figure B4-3. ARMM OFR Word

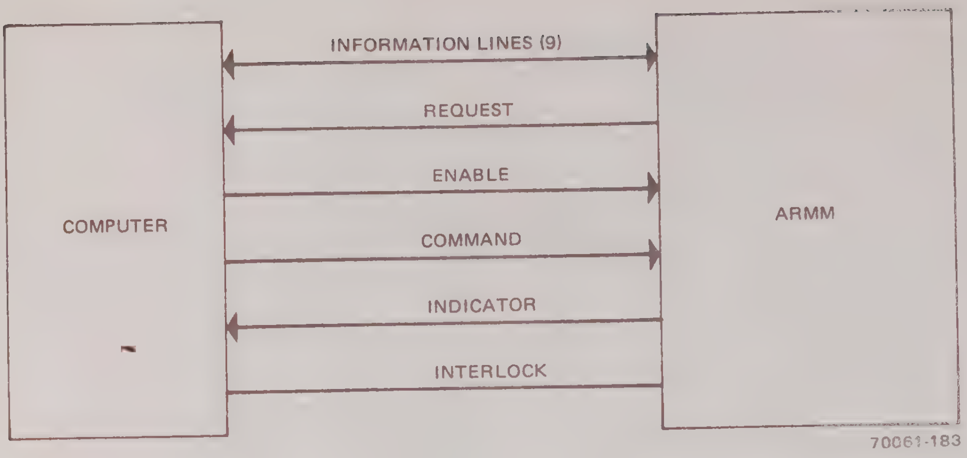

INFORMATION LINES (9)
REQUEST
ENABLE
COMMAND
INDICATOR
INTERLOCK
COMPUTER
ARMM
70061-183

Figure B4-2. ARMM Computer Interface

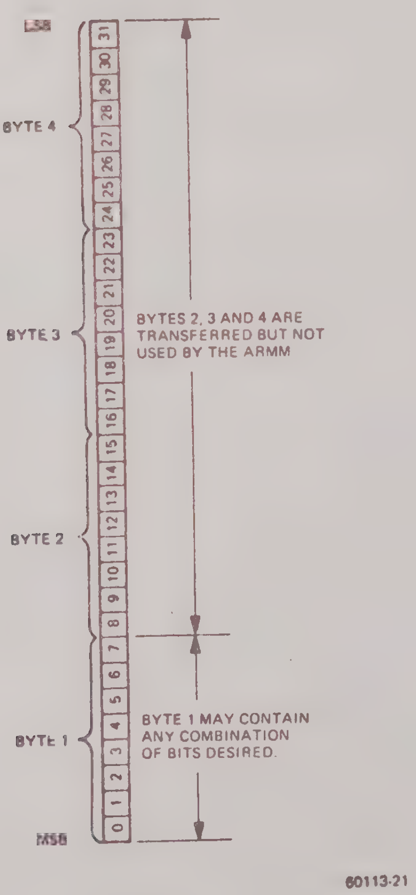
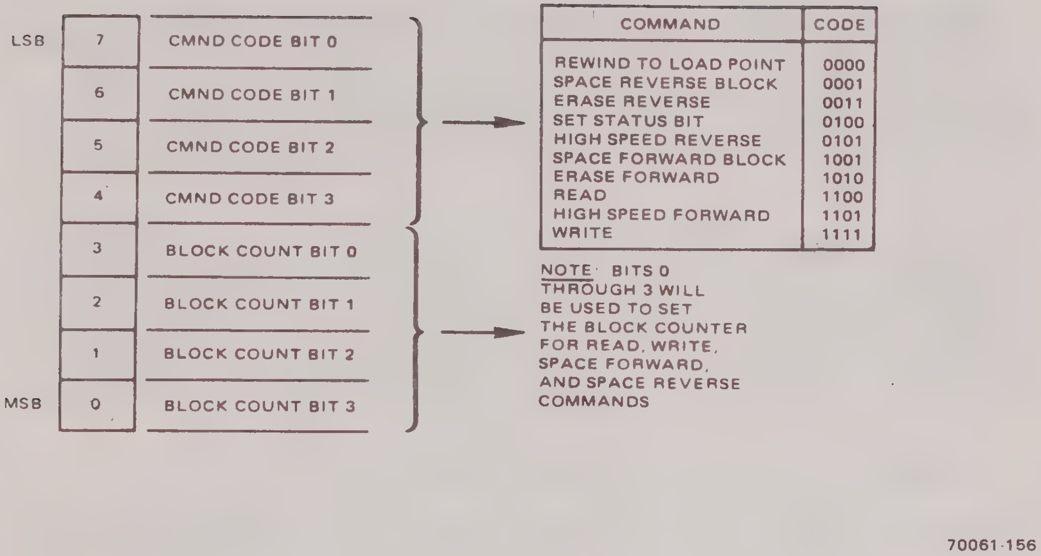

LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
BYTES 2, 3 AND 4 ARE TRANSFERRED BUT NOT USED BY THE ARMM
BYTE 1 MAY CONTAIN ANY COMBINATION OF BITS DESIRED.
60113-21

Figure B4-3. ARMM OFR Word


LSB
7
CMND CODE BIT 0
6
CMND CODE BIT 1
5
CMND CODE BIT 2
4
CMND CODE BIT 3
3
BLOCK COUNT BIT 0
2
BLOCK COUNT BIT 1
1
BLOCK COUNT BIT 2
MSB
0
BLOCK COUNT BIT 3
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COMMAND	CODE
REWIND TO LOAD POINT	0000
SPACE REVERSE BLOCK	0001
ERASE REVERSE	0011
SET STATUS BIT	0100
HIGH SPEED REVERSE	0101
SPACE FORWARD BLOCK	1001
ERASE FORWARD	1010
READ	1100
HIGH SPEED FORWARD	1101
WRITE	1111

NOTE: BITS 0 THROUGH 3 WILL BE USED TO SET THE BLOCK COUNTER FOR READ, WRITE, SPACE FORWARD, AND SPACE REVERSE COMMANDS

Figure B4-4. Device Command Byte

B4-7. ARMM Interrupts

The ARMM generates an interrupt as a result of receipt of an EOB command or detection of any of the conditions defined in the interrupt byte. The interrupt byte format is illustrated in figure B4-8 and explained in figure B4-9.

B4-8. ARMM Data Structure

Actual data transfers to and from the ARMM occur only during read or write operations. Data is transferred on a byte basis with the format shown in figure B4-10 at the interface. No fixed data structure is required for ARMM data. The only considerations are core availability and the maximum record size of 32,768 bytes (equivalent to 8192 32-bit words).

B4-9. ARMM Special Considerations

When using the loop test feature of the ARMM, a one-word buffer must be provided to accept the returned data byte. This requires the setup of a keyword and termination word for the device channel prior to executing the OFR instruction.

de	Description
0000	Rewind to Load Point. The MTA moves the tape in the reverse direction at high speed to the BOT and initiates a stop sequence and an interrupt sequence.
0001	Space Reverse. This command is identical to the space forward command except for direction. If another space reverse or erase reverse command is received within 5 milliseconds, the tape does not stop; otherwise a stop sequence is initiated.
0011	Erase Reverse. The MTA moves the tape in the reverse direction at normal speed and erases an entire data record. This command makes it possible to remove a record of data without affecting the data recorded on either side of that record. An interrupt sequence is initiated upon detection of the inter-record gap (IRG) preceding the record being erased. If another erase reverse or space reverse command is received within 5 milliseconds, the tape does not stop; otherwise a stop sequence is initiated.
0100	Set Status Bit. This command sets the ARMM status bit.
0101	High Speed Reverse. This command is identical to the high speed forward except for direction. A stop sequence is initiated when an EOB command is received or when the BOT is detected. No Interrupt sequence is initiated upon detection of the BOT, or upon detection of an error while in the Alarm mode. The Interrupt is inhibited even if an error condition occurs during this mode.
1001	Space Forward. The MTA moves the tape forward at normal speed, detects the IRG, and initiates an interrupt sequence. No data is transferred. Bits 0 through 3 of the command byte specify the number of IRGs to be disregarded (counted) before an interrupt is initiated. This allows the space forward of up to 16 records while requiring the processing of only a single interrupt. If another space forward or read command is received within 5 milliseconds the tape does not stop; otherwise a stop sequence is initiated. The tape stops with the heads positioned in the IRG.
1010	Erase Forward. The MTA moves the tape forward at normal speed and erases a fixed length of tape each time the command is issued. The length of tape erased is approximately 2 inches. No data is transferred. An interrupt sequence is initiated to notify the computer that the operation is complete. If another erase forward command is received within 5 milliseconds, the tape does not stop; otherwise a stop sequence is initiated. This command is used to erase a record in which an error occurred when it was written.
1100	Read. The MTA moves the tape forward at normal speed and transfers to the computer all the bytes in the record (unless transmission is terminated by the computer before all are read), except the longitudinal redundancy check (LRC) character. As with the write command, bits 0 through 3 of the command byte are used to specify the number of EOB commands to be disregarded. The

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Figure B4-5. ARMM Device Command Codes (Sheet 1 of 2)

Code	Description
	read operation is terminated when an EOB command is received with the block counter equal to zero, or by detection of the IRG. An interrupt sequence is initiated upon detection of the IRG or a timing error. If another read or space forward command is received within 5 milliseconds, the tape continues without stopping; otherwise a stop sequence is initiated. The tape stops with the heads positioned in the IRG.
1101	High Speed Forward. The MTA moves the tape forward at high speed and transmits a request upon detection of an IRG. Bits 0 through 3 of the command byte are ignored for all high-speed commands. A stop sequence is initiated when an EOB command is received or the EOT is detected. No interrupt sequence is initiated upon detection of the EOT. No data is transferred for any of the high-speed commands. The Interrupt is inhibited even if an error condition occurs during this mode. NOTE: The computer counts the requests in the alarm mode and issues an EOB when the block length field of the I/O key word is decremented to zero. The high-speed start or stop distance is approximately 4.5 inches. This means that the tape will not necessarily stop with the heads positioned in an IRG. Also, during a high-speed start or stop, very short records may not be detected. Consequently, the exact position of the tape can be determined only by reading the record identification at normal speed.
1111	Write. The MTA moves the tape forward at normal speed; writing continues as long as the computer supplies bytes at the rate requested by the MTA. Bits 0 through 3 of the command byte specify the number of EOB commands to be disregarded (counted) by the MTA. When an EOB is received with the block counter equal to zero, a write terminate operation is initiated. The write terminate operation consists of encoding and writing the LRC character, generating the inter-record gap (IRG), and initiating an interrupt sequence. If a byte is not available from the computer at the write strobe time, a timing error is detected and a write terminate operation is initiated. If another write or erase command is received within 5 milliseconds, the tape continues without stopping; otherwise a stop sequence is initiated. The data recorded on tape is organized into logical groups called records. The records length is determined by the block length field of the I/O keyword (in the computer) and the block length field of the Device command byte (in the computer). The maximum record length can be 2048 x 16 bytes. This is equivalent to 8192, 32-bit computer words and requires approximately 54.6 inches of tape. Because the number and length of the records on a given tape are both variable, some means of positively locating a desired record is rerequired. For positive location, the first two or more bytes of each record, to be determined by software design will contain a record identified.

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Figure B4-5. ARMM Device Command Codes (Sheet 2 of 2)

LSB	7	MOTOR ERROR
	6	EOT
	5	NO DATA
	4	STATUS
	3	BOT
	2	WRITE ENABLED
	1	BUSY
MSB	0	READY

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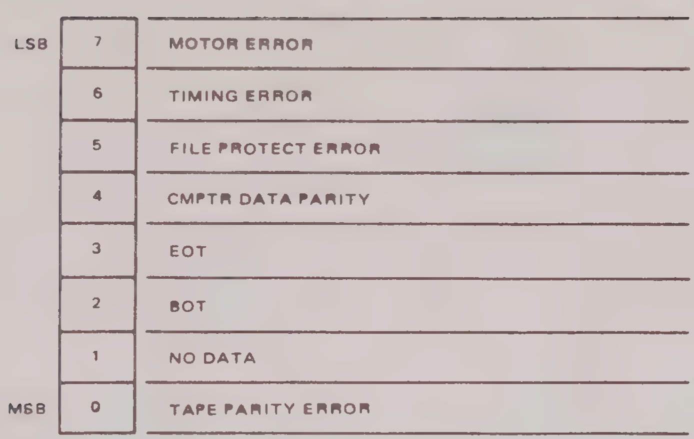
Figure B4-6. ITR Byte Format

Bit	Description
0	Ready. Indicates that the MTA is connected, power is on, unit is on-line, and the tape transport cartridge is in place.
1	Busy. Indicates that the tape unit is performing an operation.
2	Write Enabled. Indicates all write-enable controls are enabled.
3*	BOT. Indicates that a beginning-of-tape condition exists.
4	STATUS. Indicates that the tape has been repositioned by the operator.
5	No Data. Indicates that no data has been detected on the tape during a forward going operation and an amount of time equivalent to approximately 24,000 bytes has elapsed, or that no data has been detected by the read-after-write circuitry during a write operation.
6*	EOT. Indicates that an end-of-tape condition exists.
7	Motor Error. Indicates that the motor has not started by the end of the start delay.
	*Note: When both bits 3 (BOT) and 6 (EOT) are on at the same time this indicates that the tape is in the parking zone. The tape must manually be rewound off line to the BOT.

60113-25A

Figure B4-7. ITR Byte Content and Usage



60113 26

Figure B4-8. Interrupt Byte Format

Bit	Description
0	Tape Parity Error. Indicates a lateral or longitudinal (LRC) parity error was detected on tape during the previous operation.
1	No Data. Indicates that no data has been detected on the tape during a forward going operation and an amount of time equivalent to approximately 24,000 bytes has elapsed, or that no data has been detected by the read-after-write circuitry during a write operation.
2	BOT. Indicates that a beginning-of-tape condition exists.
3	EOT. Indicates that an end-of-tape condition exists.
4	Computer Data Parity Error. Indicates that a parity error has been detected in a data byte transferred from the computer during a write command.
5	File Protect Error. Indicates that a write or erase command was attempted when the MTA was not write-enabled.
6	Timing Error. Indicates that the computer did not respond with data in time for a write mode, or did not accept data in time for a read mode.
7	Motor Error. Indicates that the motor has not started by the end of the start delay.

60113-27

Figure B4-9. Interrupt Byte Content and Usage

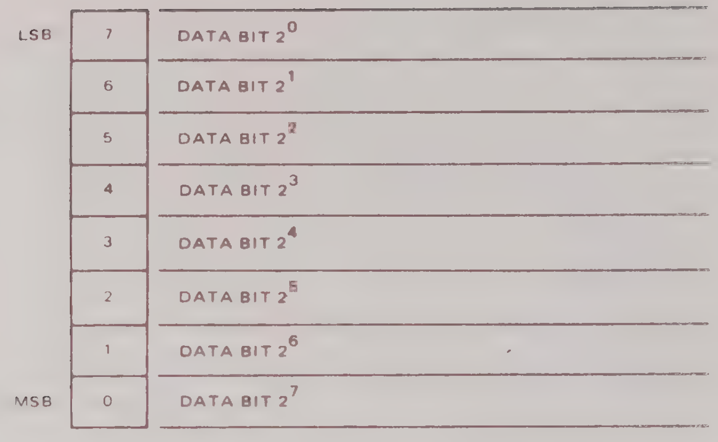


Figure B4-10. ARMM Data Byte Format

Section V. DIGITAL DATA TERMINAL

B5-1. DDT General

The digital data terminal (DDT) is used to convert computer data into a form compatible with transmission requirements for voice grade communications networks. The same unit also has the capability to receive transmissions and convert the information into a computer-compatible data format (figure B5-1).

B5-2. DDT Capabilities

The DDT may transmit and/or receive at a rate of 600 or 1200 bits per second. Automatic error correction is accomplished with added hamming bits and upon selection each block of data may be transmitted twice (sequentially). Also provided are the connections to use cryptographic devices to encode transmission and decode received data. It should be noted that all of the above are hardware controlled features.

B5-3. DDT References

DDT Development Specification EL-CP-00041109

Message and Code Standards Specification EL-SS-0004-R-3

B5-4. DDT-to-Computer Interface

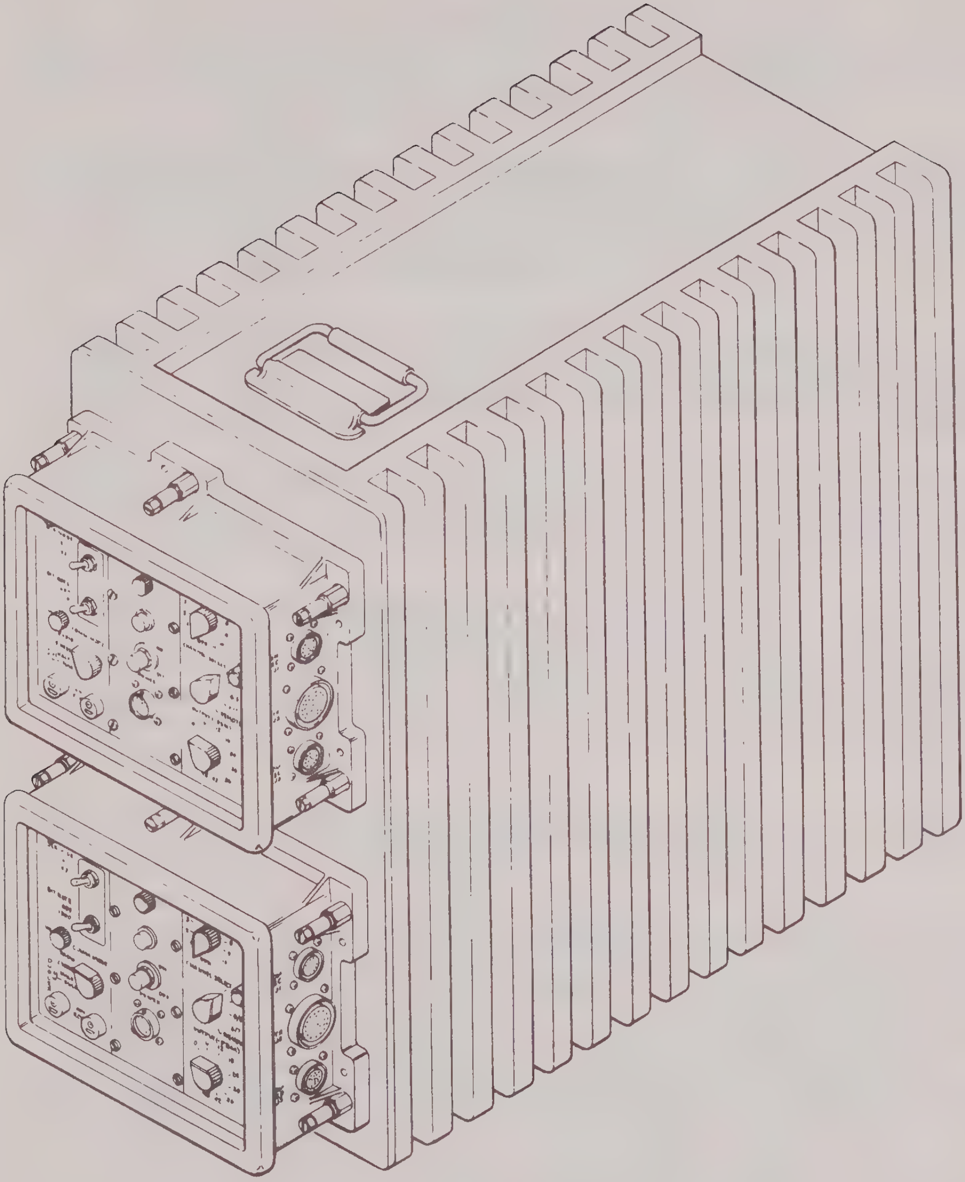
Data transfers between the computer and DDT are performed on an automatic input/output interrupt basis. Communications are on a byte to byte basis for the DDT. Due to the full duplex capability of the DDT the transmit and receive functions are assigned separate channels resulting in the use of two request lines while all other lines remain common. Figure B5-2 illustrates the interface.

B5-5. DDT Command and Control Word(s)

With the previously mentioned separate channel assignments for transmit and receive, each channel has its own control format. Overall control of the DDT is via Device commands, one set for transmit and one set for receive.

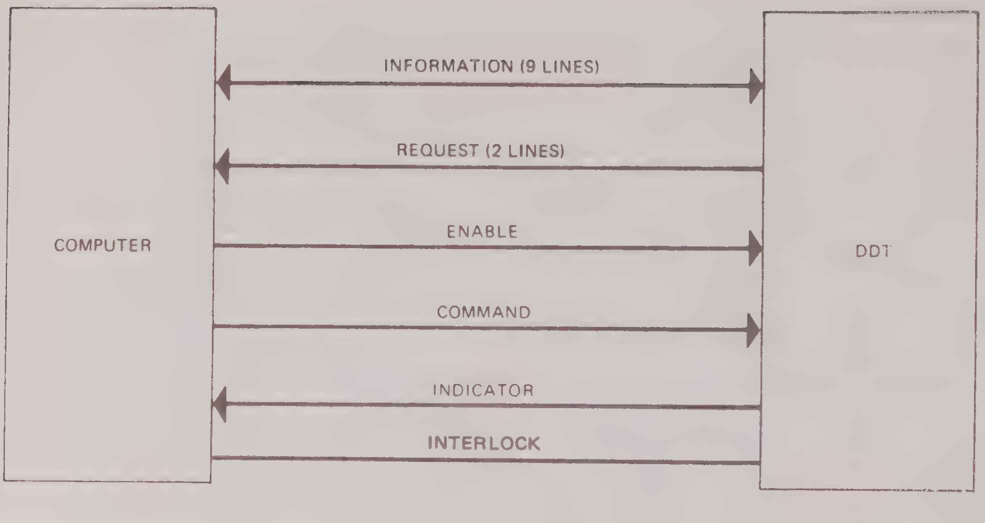
a. *Device Command Byte (Transmit).* The transmit channel commands are illustrated in figure B5-3 and their usage is defined in figure B5-4.

b. *Device Command Byte (Receive).* The receive channel commands are illustrated in figure B5-5 and their usage is defined in figure B5-6.



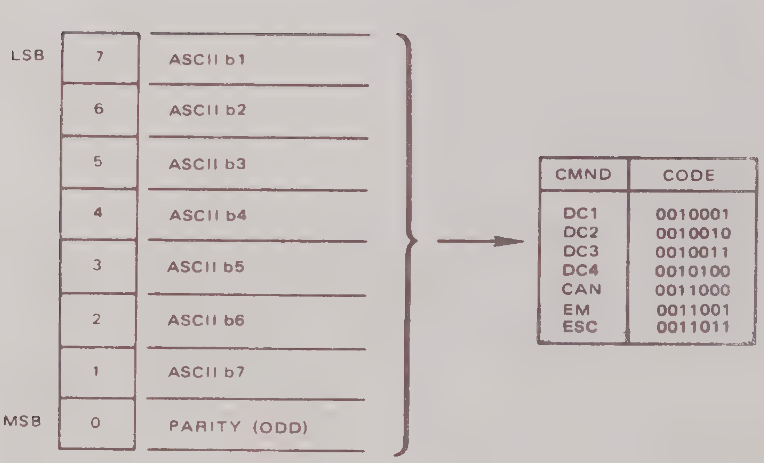
44-2-006

Figure B5-1. Data Terminal Unit (Contains Two Each DDT)


INFORMATION (9 LINES)
REQUEST (2 LINES)
COMPUTER
ENABLE
DDT
COMMAND
INDICATOR
INTERLOCK

70061-158

Figure B5-2. DDT-to-Computer Interface


LSB
7 ASCII b1
6 ASCII b2
5 ASCII b3
4 ASCII b4
3 ASCII b5
2 ASCII b6
1 ASCII b7
MSB
0 PARITY (ODD)

CMND	CODE
DC1	0010001
DC2	0010010
DC3	0010011
DC4	0010100
CAN	0011000
EM	0011001
ESC	0011011

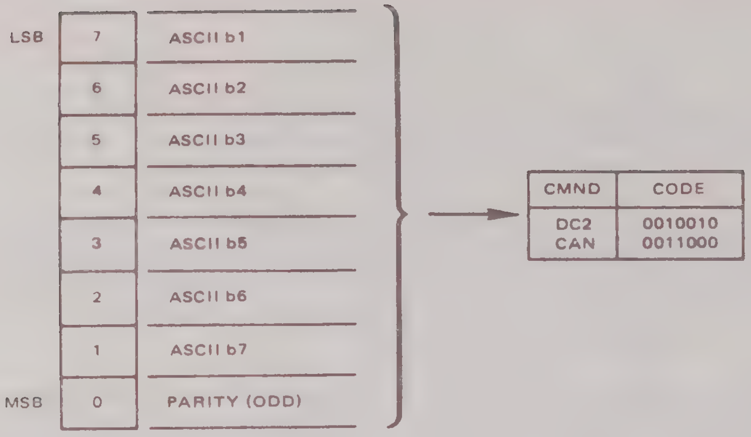
70061-159A

Figure B5-3. DDT Transmit Device Command Byte

Code	Description
001 0001	Transmit Clear Message (DC1). When this state is initiated by the controlling device, the DDT unconditionally initiates message composition and transmission (if COMSEC equipment is not connected to the DDT).
001 0010	Transmit Clear Message on Remote Command (DC2). When this state is initiated by the controlling device, the DDT generates an interrogation signal (Data Ready) for use by the DTMU*. Message composition and transmission is initiated on receipt of reply signal (Transmit) from the DTMU* (if COMSEC equipment is not connected to the DTA).
001 0011	Computer Interface Loop Test (DC3). When this state is initiated by the controlling device, the DDT connects the transmitter input interface to the receiver output interface. The DDT then initiates a request for data from the controlling device and supplies these same data back via the receiver output.
001 0100	Local Loop Test (DC4). When this state is initiated by the controlling device, the DDT connects the transmit output directly to the receive input and initiates message composition and transmission. This test is not operative if a half-duplex KG is connected.
001 1000	Cease Transmission of Preamble (CAN). When this state is initiated by the controlling device (after a DC1, DC2, or ESC command to transmit) prior to completion of transmission of the message preamble, the transmission state is terminated and the transmit channel is returned to standby. If received after transmission of the message preamble, the command is ignored and the transmission is continued.
001 1001	Transmit Secure Message without DTMU Control (EM). If COMSEC equipment is not connected (processor connected offline encryption), the data is transmitted in the store-and-Forward Mode.
001 1011	Transmit Secure Message on Remote Command (ESC). When this state is initiated by the controlling device, the DDT generates an interrogation signal (Data Ready) for use by the DTMU*. Message composition and transmission is initiated on receipt of the reply signal (Transmit) from the DTMU*. If COMSEC equipment is connected to the DDT, the data is processed through the COMSEC equipment (encrypted), prior to transmission. If COMSEC equipment is not connected (processor connected offline encryption), the data is transmitted in the store-and-forward mode.
	*DTMU function may also be performed by CCU.

70061-160

Figure B5-4. Transmit Device Command Content and Usage


LSB
7
ASCII b1
6
ASCII b2
5
ASCII b3
4
ASCII b4
3
ASCII b5
2
ASCII b6
1
ASCII b7
MSB
0
PARITY (ODD)
CMND
CODE
DC2
CAN
0010010
0011000

70061-252

Figure B5-5. DDT Receive Device Command Byte

Code	Description
001 0010	DC2, Begin receiving. This command activates the DTA receive section after it has been deactivated by the Master Reset or CAN command.
001 1000	CAN, Cease receiving. This causes the receive section to cease sending requests to the computer.

60113-34

Figure B5-6. Receive Device Command Content and Usage

LSB	7	DTA IS RECEIVING A MESSAGE
	6	600 BAUD OPERATION
	5	DTA IS IN SINGLE BLOCK TRANSMISSION MODE
	4	DTMU IS INHIBITING TRANSMISSION
	3	KEY GENERATOR CONNECTED
	2	DTA IS IN SEND MODE
	1	RECEIVE TRANSFER ERROR OR TIME-OUT
MSB	0	TRANSMIT TRANSFER ERROR OR TIME-OUT

70061-161

Figure B5-7. ITR Status Byte

B5-6. DDT Status Word(s)

Device status information is returned to the computer from the DDT transmit or receive channels in the form of an ITR word, consisting of one 8-bit byte, when an ITR command is issued by the computer. Although an ITR may be initiated on the receive or transmit channel, the ITR Status Byte (figure B5-7) returned to the computer will be identical in all respects.

NOTE

The error bit, if set, will be reset for the channel that was interrogated.

B5-7. Interrupts

An interrupt is generated by the DDT after the received message EOT sequence is detected signifying the end of that message. No information is transferred with this interrupt. Also there is no interrupt generation for the transmit channel.

B5-8. DDT Data Structures

Data is transferred between the computer and DDT on a byte by byte basis with each byte representing an ASCII character. There are no hardware limitations on the number of bytes/characters that may be transferred, only core requirements and system tolerances cause any limitations.

B5-9. DDT Special Considerations

When using the computer interface loop test feature of the DDT, a buffer must be provided for the receive channel data. This requires setup of a keyword and termination word plus I/O initiation for the receive channel.

Section VI. DIGITAL PLOTTER MAP

B6-1. DPM General

The digital plotter map (DPM) provides for graphic display of topographic and tactical information under computer control (figure B6-1). The DPM allows plotting of lines, characters, and symbols on maps or overlays, to depict various situations. The graphic capability is as follows:

a. Lines, grids, and irregularly shaped areas with associated alphanumerics.

b. Special symbols as required by the particular application.

The DPM also may be used manually to transfer coordinates to the computer and to draw various shapes/lines under operator control.

B6-2. DPM Capabilities

The DPM can generate 103 different types of symbols and alphanumerics for display on its 48 by 48 in. plotting surface. The positioning is done in X and Y coordinates originating in the lower left hand corner of the plotting area. The symbols (figures B6-2 and B6-3) and alphanumerics (figure B6-4) are generated by the DPM internally. Figure B6-5 illustrates a typical DPM

.

-3. DPM References

DPM Development Specification EL-CP-00041110

DPM Technical Manual TM 11-7440-247-35

Message and Code Standards Specification EL-SS-0004-R-3

B6-4. DPM-to-Computer Interface

Data transfers between the computer and DPM are performed on an automatic input/output and interrupt basis. Communications is on a 32-bit word basis with actual data transfers being accomplished via 8-bit bytes using nine information lines (8 data and 1 parity) and four additional control lines, as illustrated by figure B6-6.

B6-5. DPM Command and Control Word(s)

Control of the DPM presentation by the computer is accomplished using four types of command words. Their format and purpose are defined in the following paragraphs and figures.

a. *OFR Word (figures B6-7 and B6-8).* An OFR command is transferred to the DPM once at the start of the DPM write cycle (OF instruction for DTM is executed).

b. *Control Word (figures B6-9 and B6-10).* A trol word is sent to the DPM for each site/word group. It basically controls plotting of the special symbols.

c. *Position Word (figures B6-11 and B6-12).* One or more position words are sent to the DPM within each site/word group. The word instructs the pen where it is to be positioned in X and Y and whether the pen is to be up or down. The position is defined relative to the DPM basic reference point which is the lower left corner of the active plotting surface.

d. *Character Word (figures B6-13, B6-14 and B6-15).* Character words are used to define which characters or symbols are to be drawn. Four characters/symbols may be defined in one word along with the row-column information locating the first element within the character field matrix.

B6-6. DPM Status Word(s)

When an ITR command is issued by the computer (ITR instruction for DPM is executed). Device status information is returned to the computer from the DPM in the form of ITR words 1, 2, and 3. The actual ITR word sent is the one specified by ITR select bits in a previously transferred OFR word. The format and purpose of the ITR words are defined in the following paragraphs and figures.

a. *ITR1 Word (figures B6-16 and B6-17).* Contains status of the various switches on the plotter front panel and the status of the limit switches.

b. *ITR2 Word (figures B6-18 and B6-19).* Contains position data indicating where the plotting pen is at the time this ITR is sent (used for manual data entry).

c. *ITR3 Word (figures B6-20 and B6-21).* Contains information regarding the memory address register and the X and Y stepper counters.

B6-7. DPM Interrupts

The DPM initiates an interrupt and transfers an interrupt byte to the computer upon receipt of an EOB command from the computer. Additionally, individual interrupts are generated for any occurrence of the conditions defined in figure B6-22. Figure B6-23 defines the interrupt byte format.

B6-8. DPM Data Structures

Site and line displays consist primarily of symbols and alphanumerics. The organization of the display data is illustrated in figure B6-24. Because the data structure is only a combination of the previously defined command words, combinations other than the one shown are allowable, depending on the application.

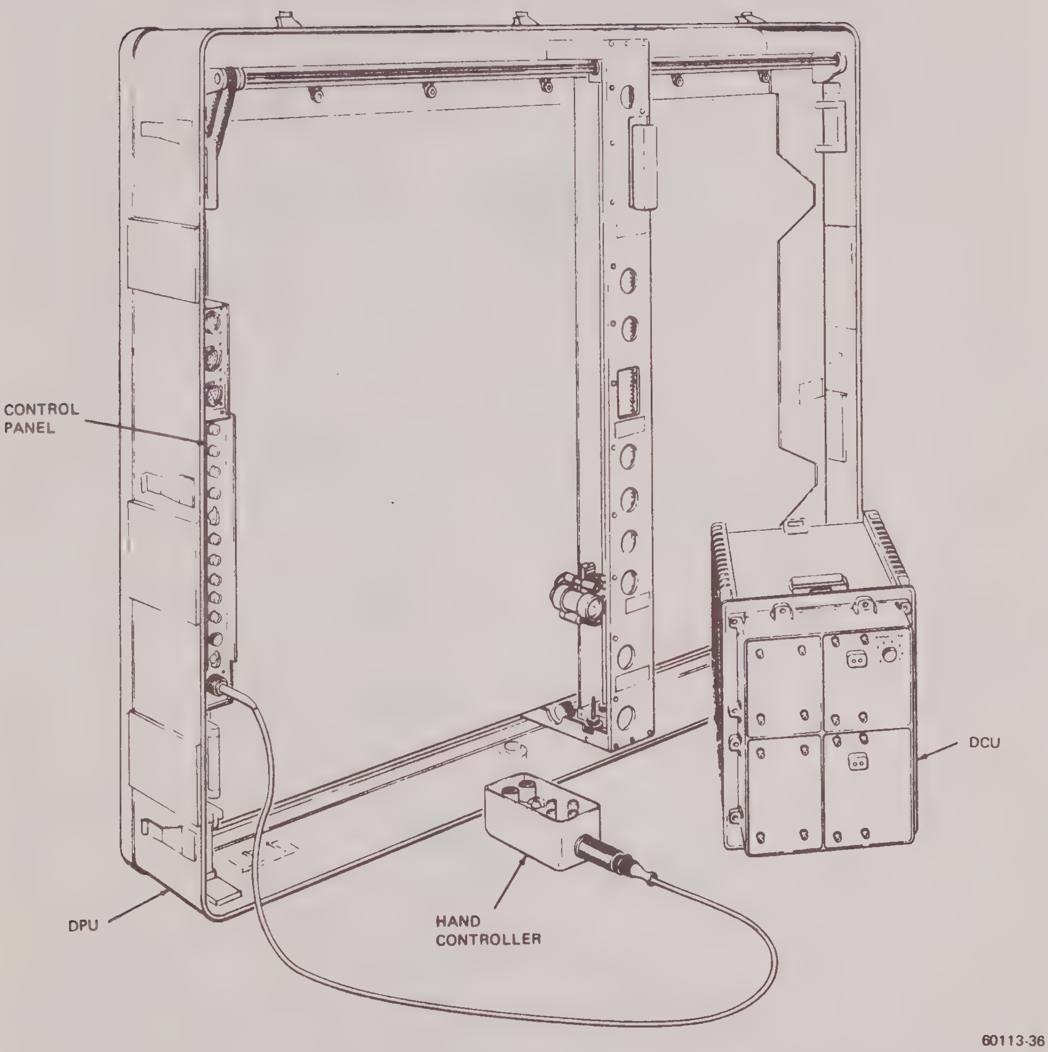
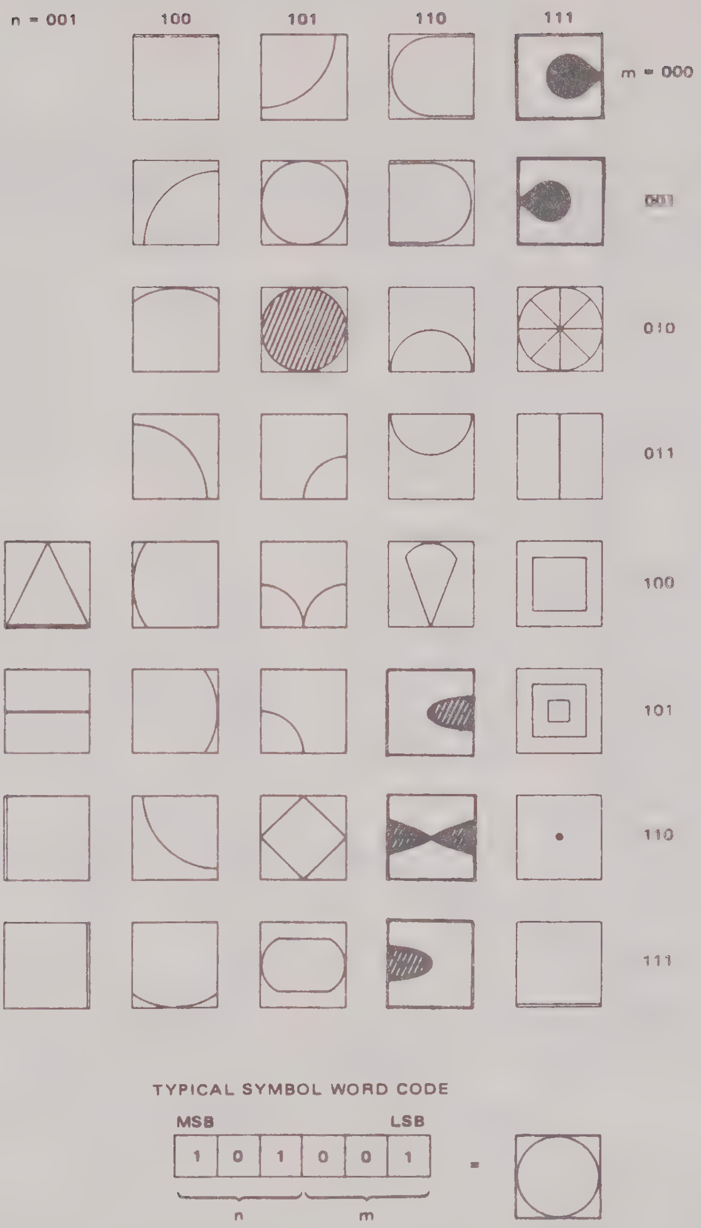

CONTROL PANEL
DCU
DPU
HAND CONTROLLER
60113-36

Figure B6-1. Digital Plotter Map


n = 001
100
101
110
111
m = 000
001
010
011
100
101
110
111
TYPICAL SYMBOL WORD CODE
MSB
LSB
1
0
1
0
0
1
=
n
m

CODE 000000 = BLANK (NO SYMBOL)

NOTE: BOX AROUND SYMBOL IS NOT PART OF SYMBOL. IT IS SHOWN HERE FOR REFERENCE ONLY.

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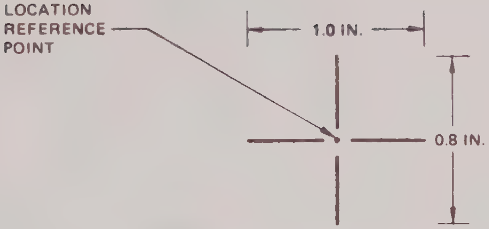
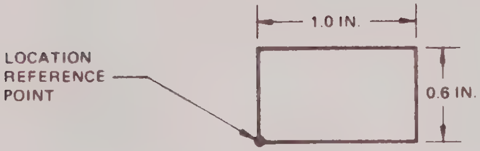
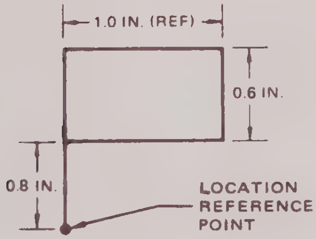
Figure B6-2. Symbol Library


LOCATION
REFERENCE
POINT
1.0 IN.
0.8 IN.

A. TARGET


1.0 IN.
LOCATION
REFERENCE
POINT
0.6 IN.

B BOX


1.0 IN. (REF)
0.6 IN.
0.8 IN.
LOCATION
REFERENCE
POINT

C BOX WITH FLAGSTAFF

70061-186

Figure B6-3. Special Symbols

Column →				0	1	2	3	4	5	6	7	Row
b7 b5						0 0	0 1	1 0	1 1			↓
b4	b3	b2	b1									
0	0	0	0			SP	0	@	P			0
0	0	0	1			!	1	A	Q			1
0	0	1	0			"	2	B	R			2
0	0	1	1			#	3	C	S			3
0	1	0	0			$	4	D	T			4
0	1	0	1			%	5	E	U			5
0	1	1	0			&	6	F	V			6
0	1	1	1			(apos)	7	G	W			7
1	0	0	0			(	8	H	X			8
1	0	0	1			)	9	I	Y			9
1	0	1	0			*	.	J	Z			10
1	0	1	1			+	,	K	[			11
1	1	0	0			,	<	L	\			12
1	1	0	1			-	=	M	]			13
1	1	1	0				>	N	∧			14
1	1	1	1			/	?	O	—			15

b7	b5	b4	b3	b2	b1	
0	0	0	1	0	0	= $
M S B					L S B	

Example of a Typical Alphanumeric Character Code

60113-39

Figure B6-4. Alphanumeric Display Character Set (64-Symbol Subset)

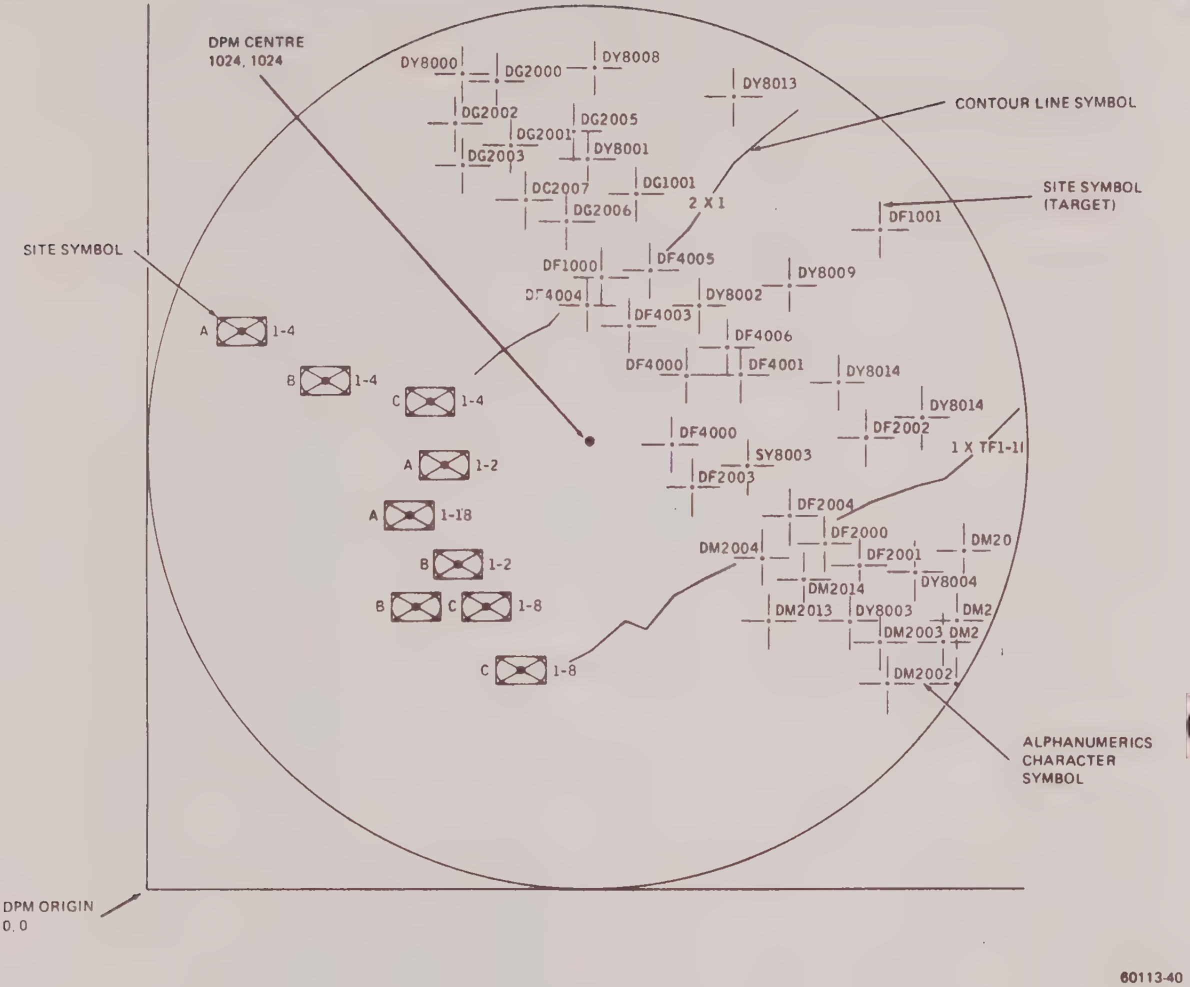
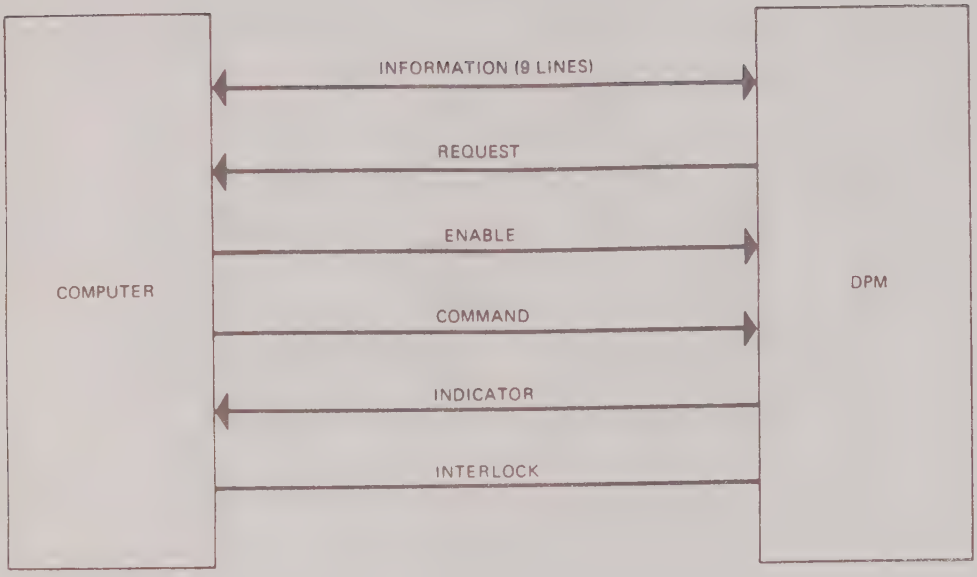

DPM CENTRE
1024, 1024
DY8000
DG2000
DY8008
DY8013
CONTOUR LINE SYMBOL
DG2002
DG2005
DG2001
DY8001
DG2003
DC2007
DG1001
2 X 1
DG2006
SITE SYMBOL
(TARGET)
DF1001
SITE SYMBOL
DF1000
DF4005
DY8009
DF4004
DY8002
DF4003
DF4006
A
1-4
B
1-4
C
1-4
DF4000
DF4001
DY8014
DY8014
DF2002
A
1-2
DF4000
SY8003
1 X TF1-11
DF2003
A
1-18
DF2004
DF2000
DM20
DM2004
DF2001
B
1-2
DM2014
DY8004
B
C
1-8
DM2013
DY8003
DM2
DM2003
DM2
C
1-8
DM2002
ALPHANUMERICS
CHARACTER
SYMBOL
DPM ORIGIN
0, 0
60113-40

Figure B6-5. Typical Display


INFORMATION (9 LINES)
REQUEST
ENABLE
COMMAND
INDICATOR
INTERLOCK
COMPUTER
DPM

60113-41

Figure B6-6. Computer-DPM Interface

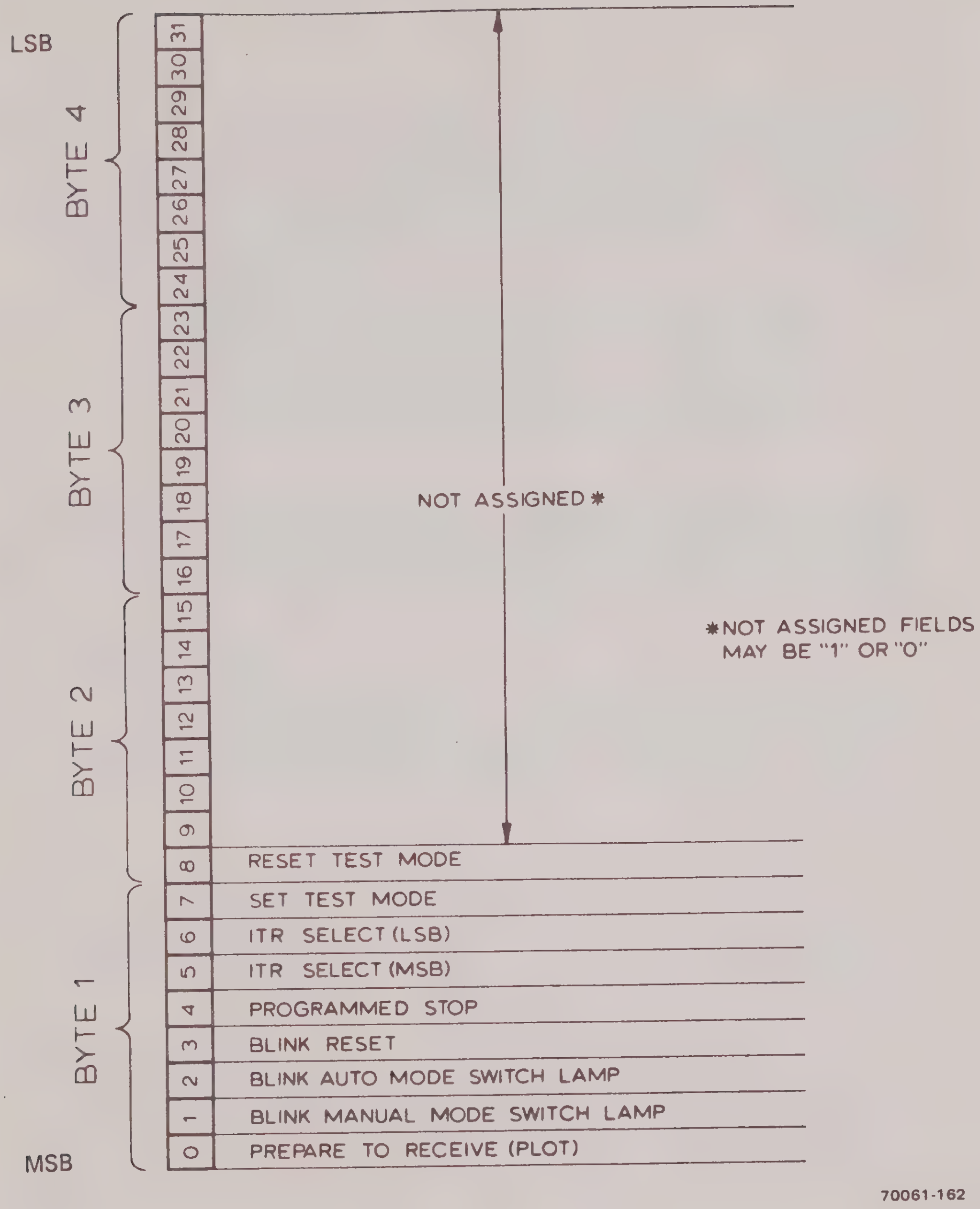

LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
NOT ASSIGNED *
*NOT ASSIGNED FIELDS MAY BE "1" OR "0"
8 RESET TEST MODE
7 SET TEST MODE
6 ITR SELECT (LSB)
5 ITR SELECT (MSB)
4 PROGRAMMED STOP
3 BLINK RESET
2 BLINK AUTO MODE SWITCH LAMP
1 BLINK MANUAL MODE SWITCH LAMP
0 PREPARE TO RECEIVE (PLOT)
70061-162

Figure B6-7. Computer to DPM OFR Word Format

Bit	Description
0	Prepare to Receive (Plot). This bit (when = 1) is used to command the DPM to start a plot sequence in accordance with the control position/line terminus, and character words to follow. Receipt of this bit sets the DPM to busy status (set ITR No. 1, bit 15 true). Busy status (ITR No. 1, bit 15) is reset by receipt of an EOB, STOP, PROGRAMMED STOP, or MASTER RESET command. NOTE: Receipt of a second OFR (prepare to receive) command prior to termination of the first OFR sequence (i.e., prior to receipt of an EOB, STOP, etc.) is an illegal command. Receipt of the second OFR will be acknowledged (indicator sent) by the DPM but the operational status of DPM will not change.
1	Blink Manual Mode Switch Lamp. This bit (when = 1) causes the Manual Mode switch lamp to blink (if the DPM is not in manual mode) and sets ITR No. 1 bit 16 true). If in the manual mode, the Manual Mode switch lamp is already illuminated and therefore will not blink; however, ITR No. 1, bit 16 is set. The ITR bit and the blink function are reset by receipt of the blink reset bit (OFR bit 3).
2	Blink Auto Mode Switch Lamp. This bit (when = 1) causes the Auto Mode lamp to blink (if the DPM is not in the Auto mode) and sets ITR No. 1, bit 17 true. If in the auto mode, the Auto Mode switch lamp is already illuminated and therefore will not blink; however, ITR No. 1, bit 17 is set. The ITR bit and the blink function are reset by receipt of the blink reset bit (OFR bit 3).
3	Blink Reset. This bit (when = 1) resets the blink auto and blink manual functions and the associated ITR bits (see bits 1 and 2 descriptions above).
4	Programmed Stop. This bit (when = 1) causes data sequence termination the same as the EOB or STOP commands. The busy status (and ITR No. 1, bit 15) is reset and an interrupt is initiated.
5, 6	ITR Select. These bits set the DPM ITR "pointer" to designate the ITR word (5, 6 = 0.1 represents ITR No. 1;5.6 = 1.0 represents ITR No. 2;5.6 = 1.1 represents ITR No. 3) to be sent to the computer in response to an ITR command.

60113-43-1

Figure B6-8. OFR Word Content and Usage (Sheet 1 of 2)

Bit	Description
7	Set Test Mode. This bit (when = 1) places the DPM in the test mode. In this mode, the DPM interrupts the computer during plotting each time one of the following occur: a. Change in data register. A change in the Y down counter or X down counter. b. Proximity signal. An interrupt shall be generated for every fourth proximity signal. NOTE: The proximity signal is utilized only during plot (pen down) of 45° lines in auto mode. During slew (pen-up) or plot of -x, -x, + Y, or -Y lines, the proximity signal is not utilized and therefore no interrupt is generated.
8	Reset Test Mode. This bit (when = 1) resets the DPM test mode (see bit 7 description above).
9-31	Not assigned.

60113-43-2

Figure B6-8. OFR Word Content and Usage (Sheet 2 of 2)

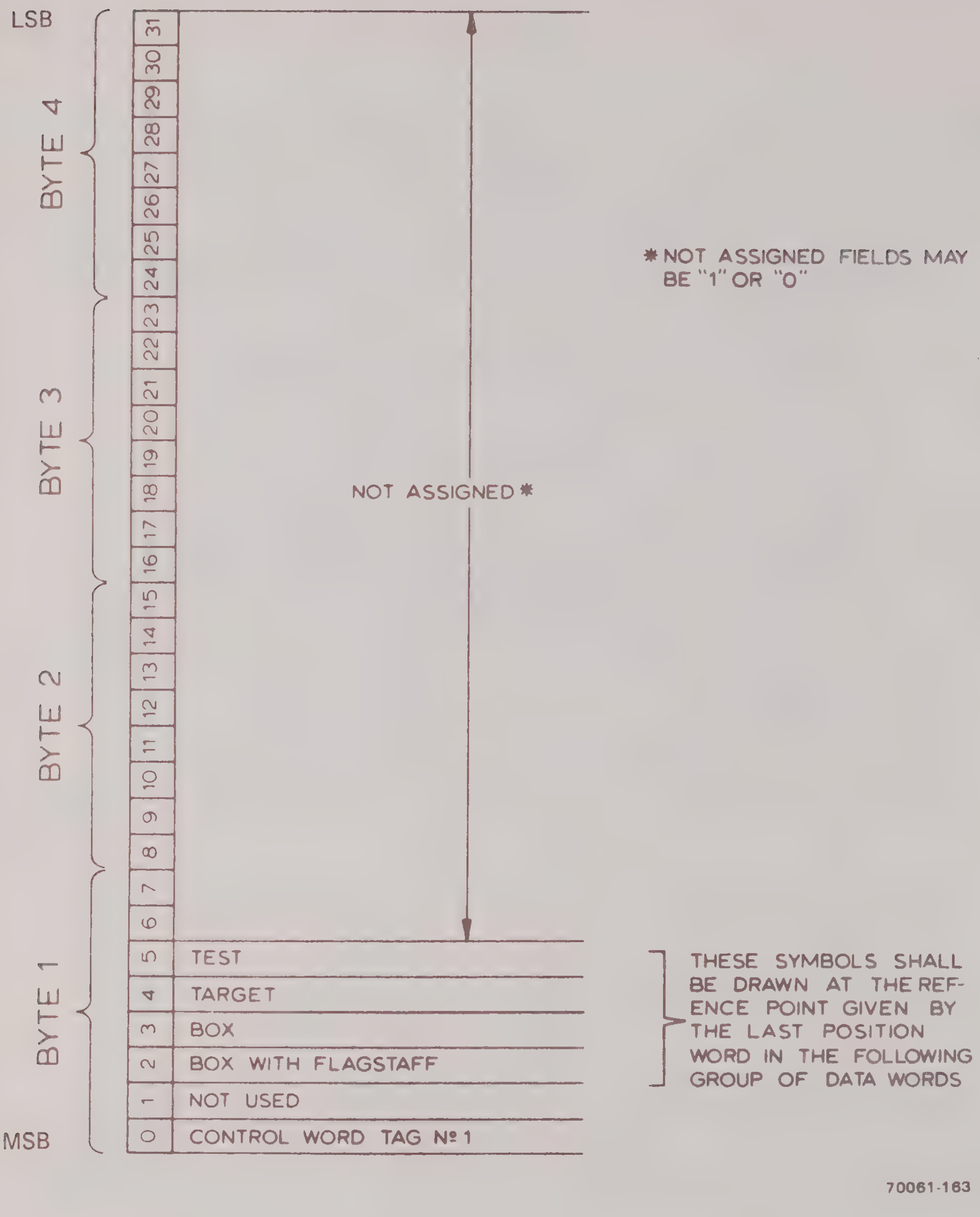
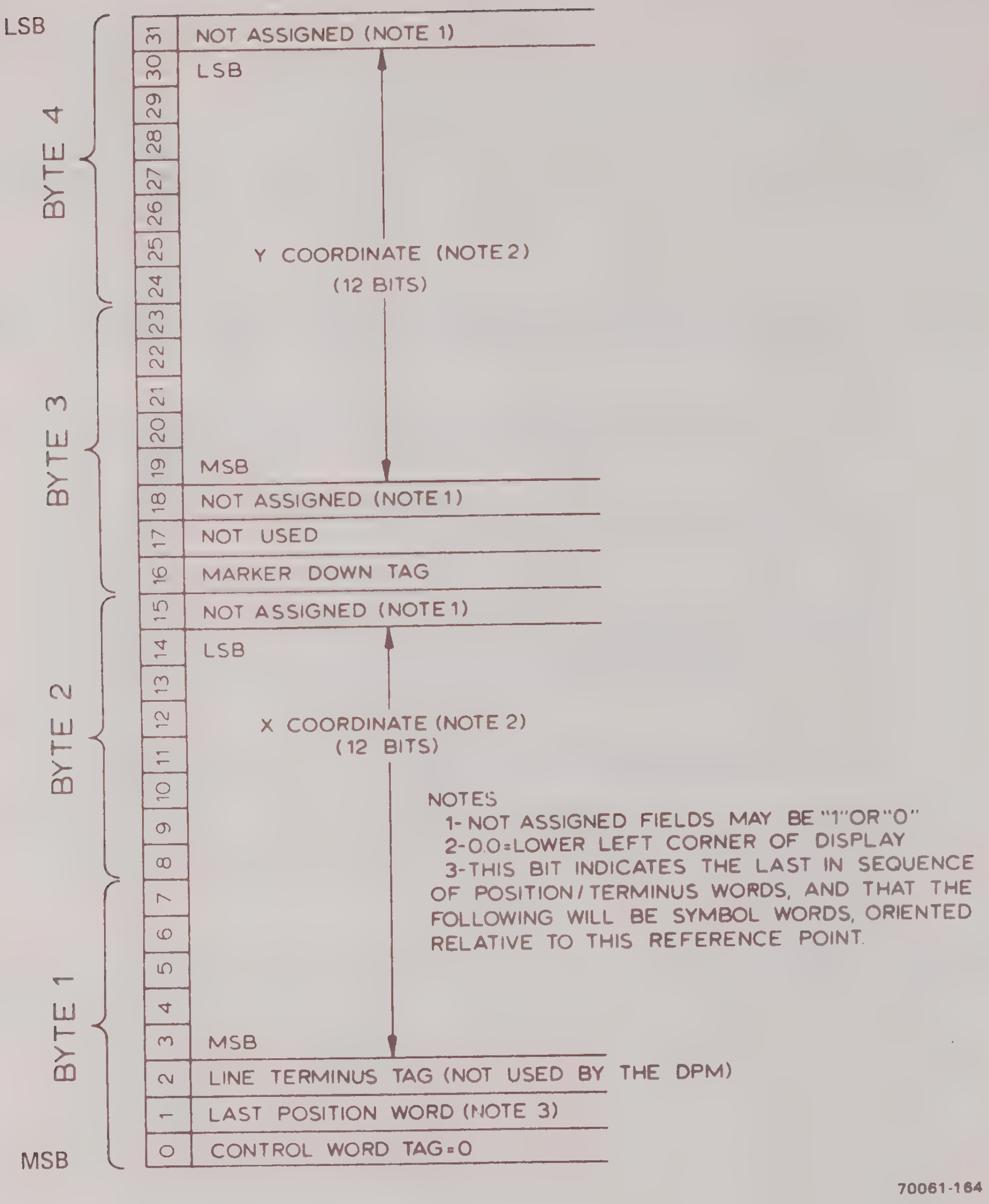

LSB
MSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
NOT ASSIGNED ✱
TEST
TARGET
BOX
BOX WITH FLAGSTAFF
NOT USED
CONTROL WORD TAG Nº 1
✱ NOT ASSIGNED FIELDS MAY BE "1" OR "0"
THESE SYMBOLS SHALL BE DRAWN AT THE REFENCE POINT GIVEN BY THE LAST POSITION WORD IN THE FOLLOWING GROUP OF DATA WORDS
70061-163

Figure B6-9. Computer to DPM Control Word Format

Bit	Description
0	Control Word Tag. This bit (when = 1) identifies the data as a control word.
1	Not used.
2	Box With Flagstaff. This bit (when = 1) causes a box with flagstaff symbol to be plotted at the location specified by the "last position" word in the data words to follow.
3	Box. This bit (when = 1) causes a box symbol to be plotted at the location specified by the "last position" word in the data words to follow.
4	Target. This bit (when = 1) causes a target symbol to be plotted at the location specified by the "last position" word in the data words to follow.
5	Test. This bit (when = 1) inhibits the marker from being placed on the plotting surface (marker down) while performing position/line terminus and character word commands associated with that control word. The plotter performs all sequences, interrupts, etc., as though it was plotting, but the pen is raised during these sequences. NOTE: This function allows the computer program to exercise the DPM through any plot sequence, without marking over existing plots. When this bit is not set (= 0) the DPM plots (marker down as commanded by position/line terminus words and character/symbol plot sequence) in the normal manner.
6-31	Not assigned.

60113-45

Figure B6-10. Control Word Content and Usage


LSB
MSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
31 NOT ASSIGNED (NOTE 1)
30 LSB
19 MSB
Y COORDINATE (NOTE 2)
(12 BITS)
18 NOT ASSIGNED (NOTE 1)
17 NOT USED
16 MARKER DOWN TAG
15 NOT ASSIGNED (NOTE 1)
14 LSB
X COORDINATE (NOTE 2)
(12 BITS)
3 MSB
2 LINE TERMINUS TAG (NOT USED BY THE DPM)
1 LAST POSITION WORD (NOTE 3)
0 CONTROL WORD TAG=0
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
70061-164

NOTES
1- NOT ASSIGNED FIELDS MAY BE "1" OR "0"
2-0.0=LOWER LEFT CORNER OF DISPLAY
3-THIS BIT INDICATES THE LAST IN SEQUENCE OF POSITION/TERMINUS WORDS, AND THAT THE FOLLOWING WILL BE SYMBOL WORDS, ORIENTED RELATIVE TO THIS REFERENCE POINT.

Figure B6-11. Computer to DPM Position/Line Terminus Word Format

Bit	Description
0	Control Word Tag. This bit (= 0) identifies the data as a position/line terminus word if a "last position" word has not been received.
1	Last Position Word. This bit (when = 1) identifies the last word of a line draw sequence and indicates that the words to follow will be character (symbol) words. The X, Y coordinates of this word identify the reference point for plotting characters or symbols.
2	Line Terminus Tag. This bit (when = 1) signifies the terminus of a plotted line. NOTE: This does not signify the end of the line draw mode: i.e., additional lines may be commanded in sequence. This bit is not used by the DPM.
3-14	X Coordinate. These bits designate the end point in the X direction to which the plotter is to travel.
15	Not assigned.
16	Marker Down Tag. When this bit is true (= 1), the marker is placed in the down (draw) position while moving from the present position to the end point specified. When this bit is false (= 0), the marker is raised.
17	Not used.
18	Not assigned.
19-30	Y Coordinate. These bits designate the end point in the Y direction to which the plotter is to travel.
31	Not assigned.

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Figure B6-12. Position/Line Terminus Word Content and Usage

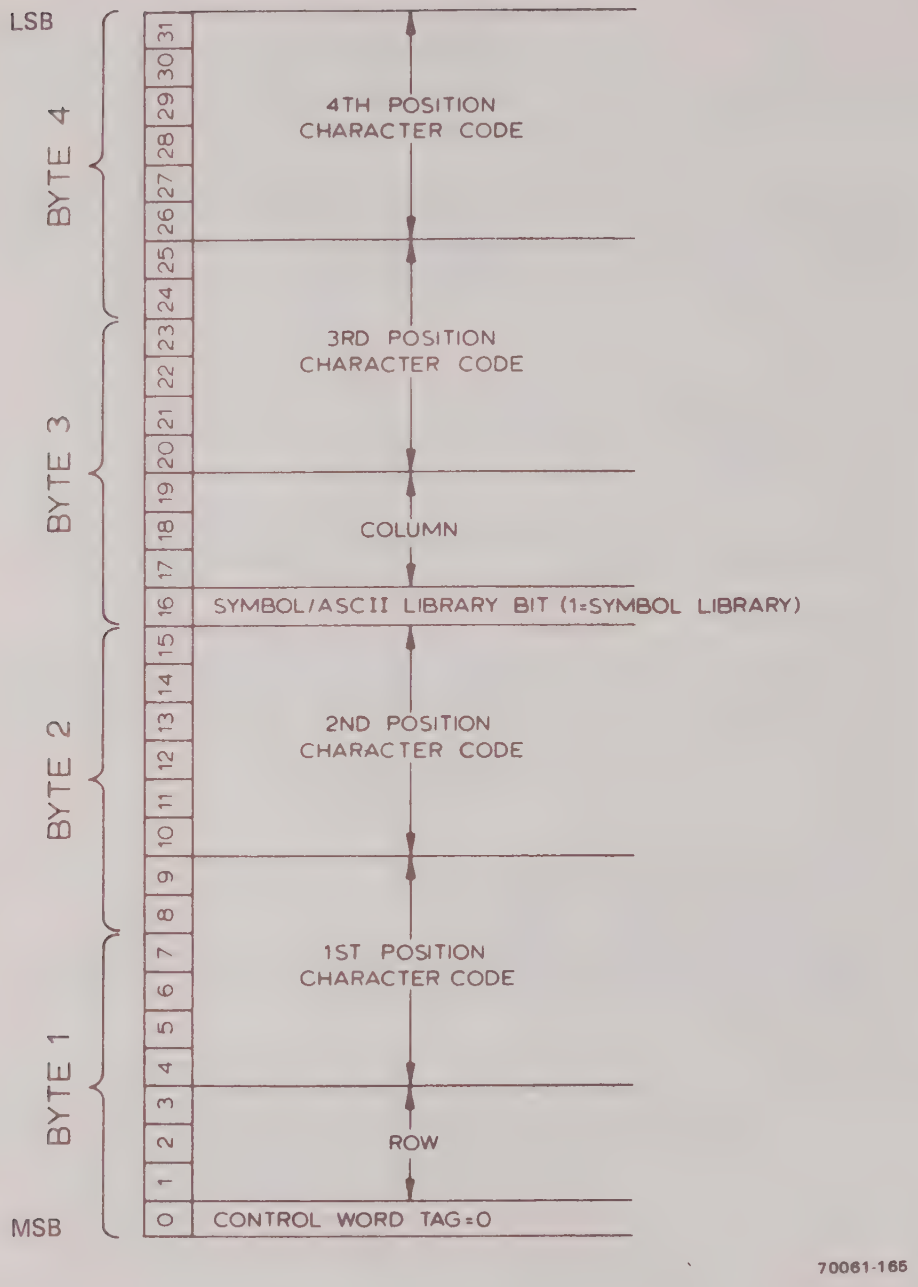
LSB
MSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
4TH POSITION CHARACTER CODE
3RD POSITION CHARACTER CODE
COLUMN
SYMBOL/ASCII LIBRARY BIT (1=SYMBOL LIBRARY)
2ND POSITION CHARACTER CODE
1ST POSITION CHARACTER CODE
ROW
CONTROL WORD TAG=0
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
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Figure B6-13. Computer to DPM Character Word Format

Bit	Description
0	Control Word Tag. This bit (= 0) identifies the data as a character word if a "last position" word has been received.
1-3	Row. These bits designate the row of the character field matrix (Figure 6-15) in which the characters or symbols are to be plotted relative to the site location reference point specified in the "last position" word.
4-9	1st Position Character Code. These bits designate the code for the character or symbol to be plotted in the first position of the character field (see Figure 6-15).
10-15	2nd Position Character Code. These bits designate the code for the character or symbol to be plotted in the second position of the character field (see Figure 6-15).
16	Symbol/ASCII Library Bit. When this bit is true (= 1), the four character codes represent symbols to be plotted. When this bit is false (= 0), the four character codes represent ASCII characters to be plotted.
17-19	Column. These bits designate the column of the character field matrix (Figure 6-15), in which the characters or symbols are to be plotted relative to the site location reference point specified in the "last position" word.
20-25	3rd Position Character Code. These bits designate the code for the character or symbol to be plotted in the third position of the character field (see Figure 6-15).
26-31	4th Position Character Code. These bits designate the code for the character or symbol to be plotted in the fourth position of the character field (see Figure 6-15).

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Figure B6-14. Character Word Content and Usage

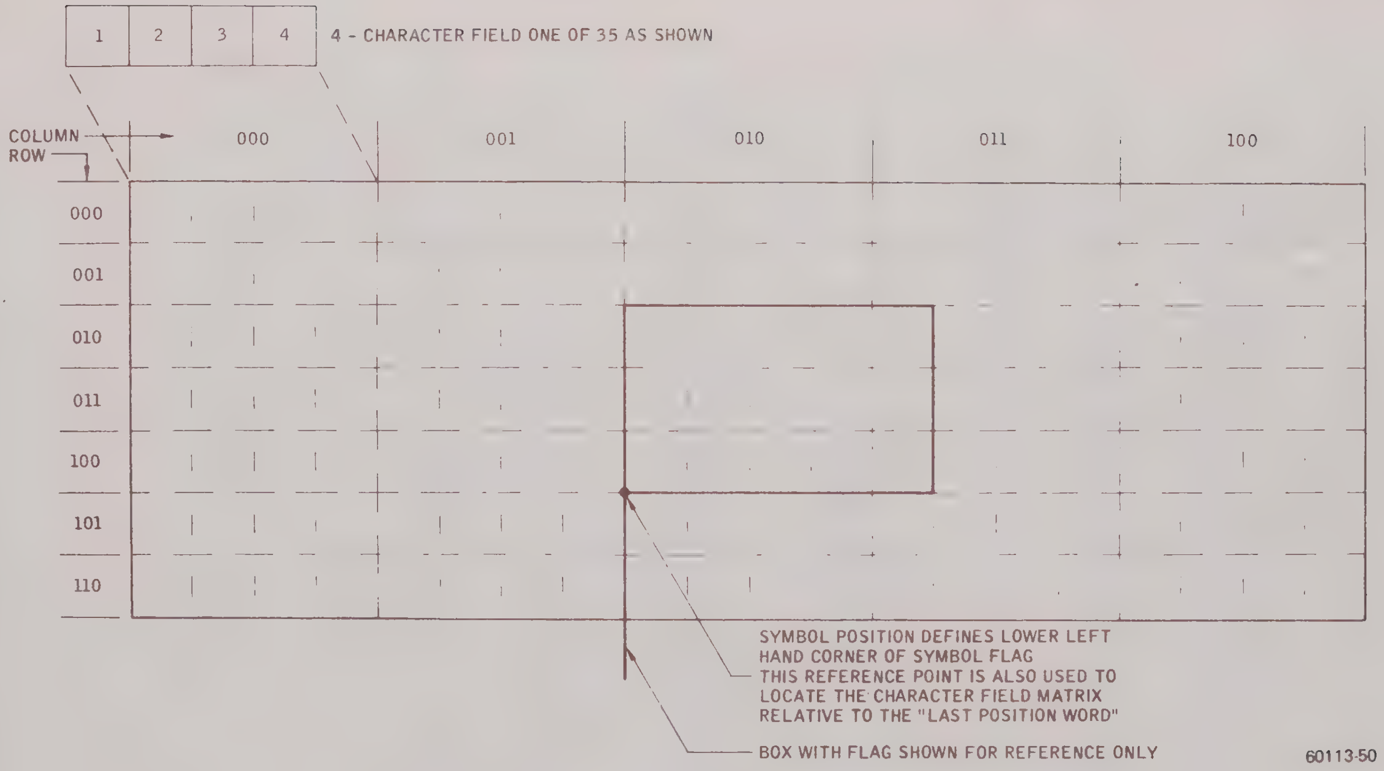
1
2
3
4
4 - CHARACTER FIELD ONE OF 35 AS SHOWN
COLUMN
ROW
000
001
010
011
100
000
001
010
011
100
101
110
SYMBOL POSITION DEFINES LOWER LEFT HAND CORNER OF SYMBOL FLAG
THIS REFERENCE POINT IS ALSO USED TO LOCATE THE CHARACTER FIELD MATRIX RELATIVE TO THE "LAST POSITION WORD"
BOX WITH FLAG SHOWN FOR REFERENCE ONLY
60113-50

Figure B6-15. Character Matrix

LSB	BYTE 4	31	NOT ASSIGNED	
		30		
		29		
		28		
		27		
		26		
		25		
		24		
	BYTE 3	23	INVERTER FAULT	(1)
		22	TEST MODE ON	
		21	-X LIMIT SWITCH INDICATOR	(1)
		20	+X LIMIT SWITCH INDICATOR	(1)
		19	-Y LIMIT SWITCH INDICATOR	(1)
		18	+Y LIMIT SWITCH INDICATOR	(1)
		17	BLINK AUTO ON	
		16	BLINK MANUAL ON	
	BYTE 2	15	BUSY (AUTO OUTPUT IN PROGRESS)	
		14	DRAW	(1) (2)
		13	STORE	
		12	DRAW / STORE SWITCH OFF	
		11	MARKER DOWN	
		10	ENTER COORD	(1) (2)
		9	MAP ALIGN	(1) (2)
		8	TEST PATTERN	(1) (2)
	BYTE 1	7	MANUAL MODE	(1)
		6	AUTO MODE	(1)
		5	NOT ASSIGNED	
		4		
		3		
		2		
		1	1 SWITCH CODE AND	
MSB		0	0 STATUS WORD ID	

NOTES
1 BITS NOTED (1) CAUSE AN INTERRUPT WHEN SET
2 BITS NOTED (2) ARE RESET BY INPUTTING ITR NUMBER 1 WORD AFTER BEING SET

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Figure B6-16. DPM to Computer (ITR) Switch Code Format (ITR Format Number 1)

Bit	Description
0-1	Switch Code and Status Word ID. These bits (bit 0 = 0, bit 1 = 1) identify the data as ITR No. 1.
2-5	Not assigned.
6	Auto Mode. This bit is true (= 1) whenever the DPM is in the automatic mode (under computer control). The DPM is placed in the auto mode by operator depression of the Auto Mode switch. The change to auto mode (from manual mode) will cause a single "status change" interrupt to be sent to the computer. The auto mode shall be reset by depression of the Manual Mode switch.
7	Manual Mode. This bit is true (= 1) whenever the DPM is in the manual mode (under operator control). The DPM is placed in the manual mode by operator depression of the Manual Mode switch. The change to manual mode (from auto mode) causes a single "status change" interrupt (see Figure 16, bit 1) to be sent to the computer. The manual mode is reset by depression of the Auto Mode switch.
8	Test Pattern. This bit is set true (= 1) when the Test Pattern switch is depressed. Depression of the Test Pattern switch causes a single "status change" interrupt to be sent to the computer. This bit is reset when the ITR No. 1 word has been sent to the computer by the DPM in response to a computer ITR command.
9	Map Align. This bit is set true (= 1) when the Map Align switch is depressed. Depression of the Map Align switch causes a single "status change" interrupt to be sent to the computer. This bit is reset when the ITR No. 1 word has been sent to the computer by the DPM in response to a computer ITR command.
10	Enter Coord. This bit is set true (= 1) when the Enter Coordinate switch is depressed and the DPM is in the manual mode. Depression of the Enter Coordinate switch (when the DPM is in the manual mode) also causes a single "status change" interrupt to be sent to the computer. This bit is reset when the ITR No. 1 word has been sent to the computer by the DPM in response to a computer ITR command.
11	Marker Down. This bit is true (= 1) whenever the marker pen is down (plot) and false (= 0) when the marker pen is up (nonplot or slew).
12	Draw/Store Switch Off. This bit is true (= 1) whenever the Line (draw/store) switch is in the off position. This bit is false (= 0) when the Line switch is in the draw or store position.

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Figure B6-17. Switch Code and Status Word (ITR Number 1) Content and Usage (Sheet 1 of 2)

Bit	Description
13	Store. This bit is true (= 1) whenever the Line switch is in the store position and false (= 0) when not in the store position.
14	Draw. This bit is set true (= 1) when the Line switch is set to the draw position and the DPM is in the auto mode. Setting the Line switch to the draw position (when the DPM is in the auto mode) causes a single "status change" interrupt to be sent to the computer. This bit is reset when the ITR No. 1 word has been sent to the computer by the DPM in response to a computer ITR command.
15	Busy. This bit is set true (= 1) by receipt by the DPM of an OFR command with the prepare to-receive bit set (see Figure 6, bit 0). This bit sets the DPM into the automatic output mode. This bit is reset when the DPM automatic output mode is reset by receipt of an EOB, STOP, PROGRAMMED STOP, or MASTER RESET command.
16	Blink Manual On. This bit is true (= 1) whenever the blink manual mode switch command has been received by the DPM. This bit is reset by receipt of the OFR blink reset bit.
17	Blink Auto On. This bit is true (= 1) whenever the blink auto mode switch command has been received by the DPM. This bit is reset by receipt of the OFR blink reset bit.
18-21	+Y, -Y, +X, -X Limit Switch Indicator. These bits are set true (= 1) when the associated limit switch is activated. Activation of any of the limit switches also shuts down the DPM inverter and cause a single "over-travel" interrupt to be sent to the computer. These bits are reset after the ITR No. 1 word has been sent to the computer and the limit switch has been deactivated.
22	Test Mode On. This bit is set true (= 1) whenever the DPM has been placed in the test mode by an OFR command. This bit is reset by receipt by the DPM of an OFR command to reset the test mode.
23	Inverter Fault. This bit is set true (= 1) when a DPM inverter shutdown (due to a fault, loss of input power, etc.) has been detected. Detection of an inverter fault shall cause a single "inverter power fault" interrupt to be sent to the computer. This bit is reset after the ITR No. 1 word has been sent to the computer and the inverter fault condition has been cleared (inverter power on).
24-31	Not assigned.

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Figure B6-17. Switch Code and Status Word (ITR Number 1) Content and Usage (Sheet 2 of 2)

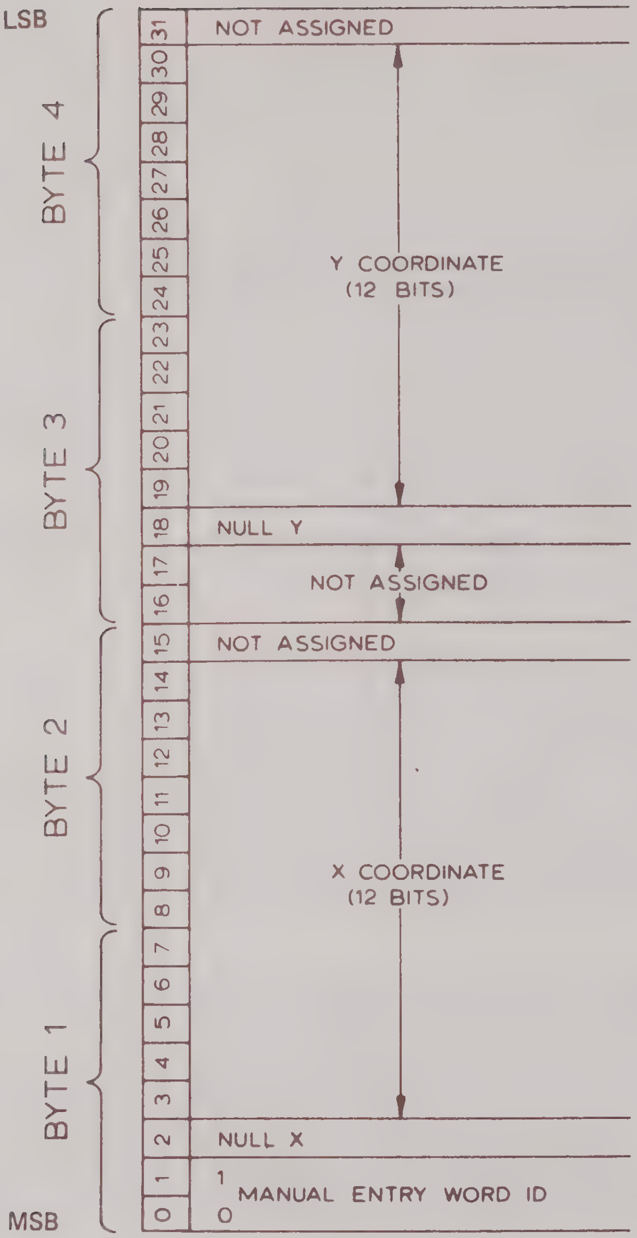
LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31 NOT ASSIGNED
30 29 28 27 26 25 24 23 22 21 20 19
Y COORDINATE (12 BITS)
18 NULL Y
17 16 NOT ASSIGNED
15 NOT ASSIGNED
14 13 12 11 10 9 8 7 6 5 4 3
X COORDINATE (12 BITS)
2 NULL X
1 1
MANUAL ENTRY WORD ID
0 0

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Figure B6-18. DPM to Computer (ITR) Manual Entry Word Format (ITR Format Number 2)

Bit	Description
0-1	Manual Entry Word ID. These bits (bit 0 = 1, bit 1 = 0) identify the data as ITR No. 2.
2	Null X. This bit shall be true (= 1) whenever an X-axis servo null condition exists (that is the actual position of the plotter arm equals the commanded position). This bit shall be false whenever the X servo is off null.
3-14	X Coordinate. These bits shall contain the present contents of the digital-to-analog (D/A) converter input register (X axis), modified by reticle displacement (X coordinate of reticle crosshair). NOTE: During slew or non 45° line plotting (+X, +Y, -X, -Y) this register shall contain the end point to which the DPM was commanded to move (after the D/A input register has been modified to the new data). During 45° line plotting, this register shall contain the incremental advance data point (DPM generated) used in conjunction with the proximity signal to plot 45° lines.
15-17	Not assigned.
18	Null Y. This bit shall be true (= 1) whenever a Y-axis servo null condition exists (that is the actual position of the plotter carriage equals the commanded position). This bit shall be false whenever the Y servo is off null.
19-30	Y Coordinate. These bits shall contain the present contents of the digital-to-analog (D/A) converter input register (Y axis), modified by reticle displacement (Y coordinate at reticle crosshair). NOTE: During slew or non 45° line plotting (+X, +Y, -X, -Y) this register shall contain the end point to which the DPM was commanded to move (after the D/A input register has been modified to the new data). During 45° line plotting, this register shall contain the incremental advance data point (DPM generated) used in conjunction with the proximity signal to plot 45° lines.
31	Not assigned.

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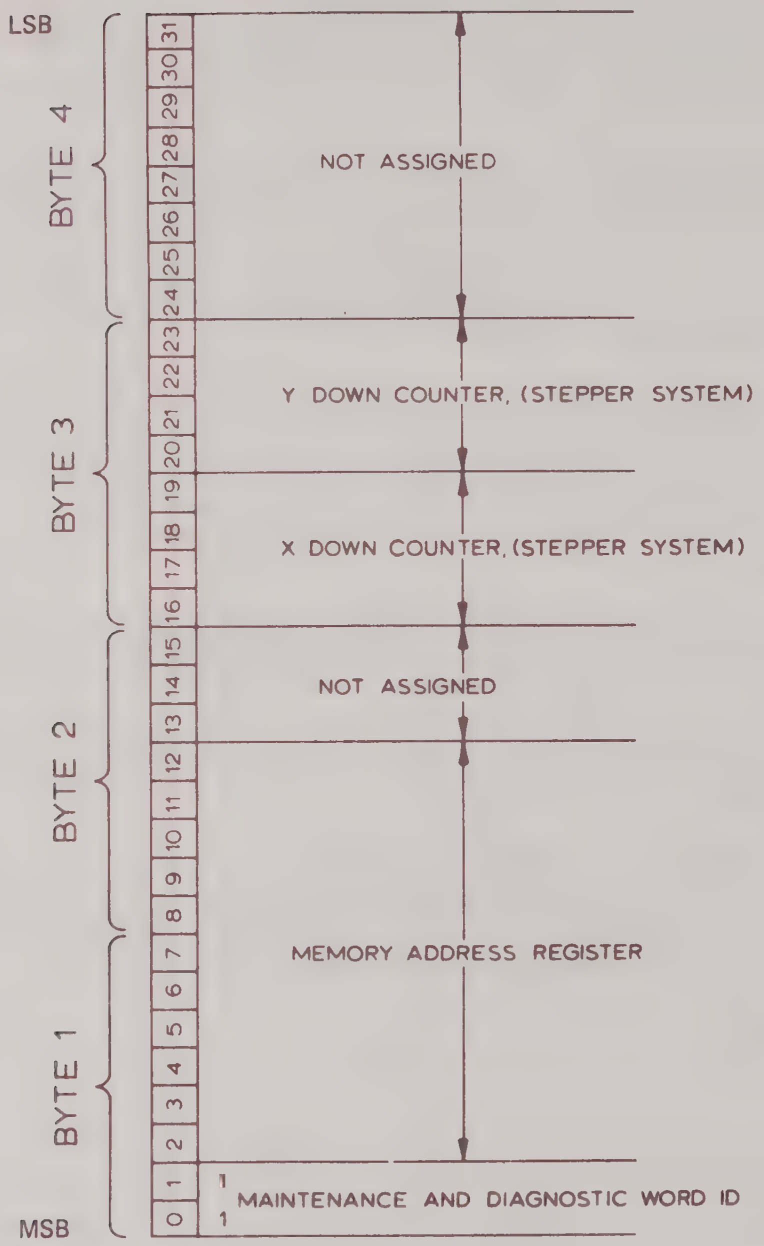
Figure B6-19. Manual Entry Word (ITR Number 2) Content and Usage


LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
NOT ASSIGNED
Y DOWN COUNTER, (STEPPER SYSTEM)
X DOWN COUNTER, (STEPPER SYSTEM)
NOT ASSIGNED
MEMORY ADDRESS REGISTER
1
1
MAINTENANCE AND DIAGNOSTIC WORD ID

70061-168

Figure B6-20. DPM to Computer (ITR) Maintenance and Diagnostic Word ID Format (ITR Format Number 3)

Bit	Description
0-1	Maintenance and Diagnostic Word ID. These bits (bit 0 = 1, bit 1 = 1) identify the data as ITR No. 3.
2-12	Memory Address Register. These bits shall equal the present contents of the DPM memory address register (memory used for plotting characters and symbols).
13-15	Not assigned.
16-19	X Down Counter. These bits shall equal the present contents of the DPM stepper system (symbol and character plotting) X down counter. When the DPM is in the test mode, each change in this register shall cause a single "change in data register" interrupt to be sent to the computer.
20-23	Y Down Counter. These bits shall equal the present contents of the DPM stepper system (symbol and character plotting) Y down counter. When the DPM is in the test mode, each change in this register shall cause a single "change in data register" interrupt to be sent to the computer.
24-31	Not assigned.

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Figure B6-21. Maintenance and Diagnostic Word (ITR Number 3)

it	Description
0	Parity Error. This bit shall be set (= 1) and an interrupt initiated whenever a parity error is detected in an OFR data word or an automatic output data word received from the computer. This bit shall be reset after the interrupt byte is transmitted to the computer.
1	Status Change. This bit shall be set (= 1) and an interrupt initiated when any one of the following switch actions occur. a. Auto Mode switch depressed. b. Manual Mode switch depressed. c. Test Pattern switch depressed. d. Map Align switch depressed. e. Enter Coord switch depressed while the DPM is in the manual mode. f. Line switch set to the draw position while the DPM is in the auto mode. This bit shall be reset after the interrupt byte is transmitted to the computer.
2	Inverter Power Fault. This bit shall be set (= 1) and an interrupt initiated when a DPM inverter shutdown (due to a fault, loss of input power, etc.) has been detected. This bit shall be reset after the interrupt byte is transmitted to the computer.
3	Overtravel. This bit shall be set (= 1) and an interrupt initiated when any of the X-Y limit switches are activated. This bit shall be reset after the interrupt byte is transmitted to the computer.
4	Proximity Signal. When the DPM is in the test mode, this bit shall be set (= 1) and an interrupt initiated each time a fourth proximity signal (applicable to 45° line plotting only) in sequence has been detected. This bit shall be reset after the interrupt byte is transmitted to the computer.
5	Change in Data Register. When the DPM is in the test mode, this bit shall be set (= 1) and an interrupt initiated for each change which occurs in the following data registers. a. Y down counter (part of stepper system used to plot characters and symbols). b. X down counter (part of stepper system used to plot characters and symbols). This bit shall be reset after the interrupt byte is transmitted to the computer.
6	Proximity Skew Excess. This bit shall be set and an interrupt initiated whenever excessive time (skew) is detected between servo proximity detections in the X and Y directions (during plotting of 45° lines). This bit shall be reset after the interrupt byte is transmitted to the computer.
7	Not assigned.

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Figure B6-22. Interrupt Byte Content and Usage

LSB	7	NOT ASSIGNED
	6	PROXIMITY SKEW EXCESS
	5	CHANGE IN DATA REGISTER (1)
	4	PROXIMITY SIGNAL (1)
	3	OVERTRAVEL
	2	INVERTER POWER FAULT
	1	STATUS CHANGE
MSB	0	PARITY ERROR

NOTES:

1. BITS NOTED (1) ARE USED ONLY WHEN THE TEST MODE IS SET.
2. ALL BITS ARE RESET AFTER TRANSMISSION OF THE INTERRUPT BYTE TO THE COMPUTER.

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Figure B6-23. DPM-to-Computer Interrupt Byte Format

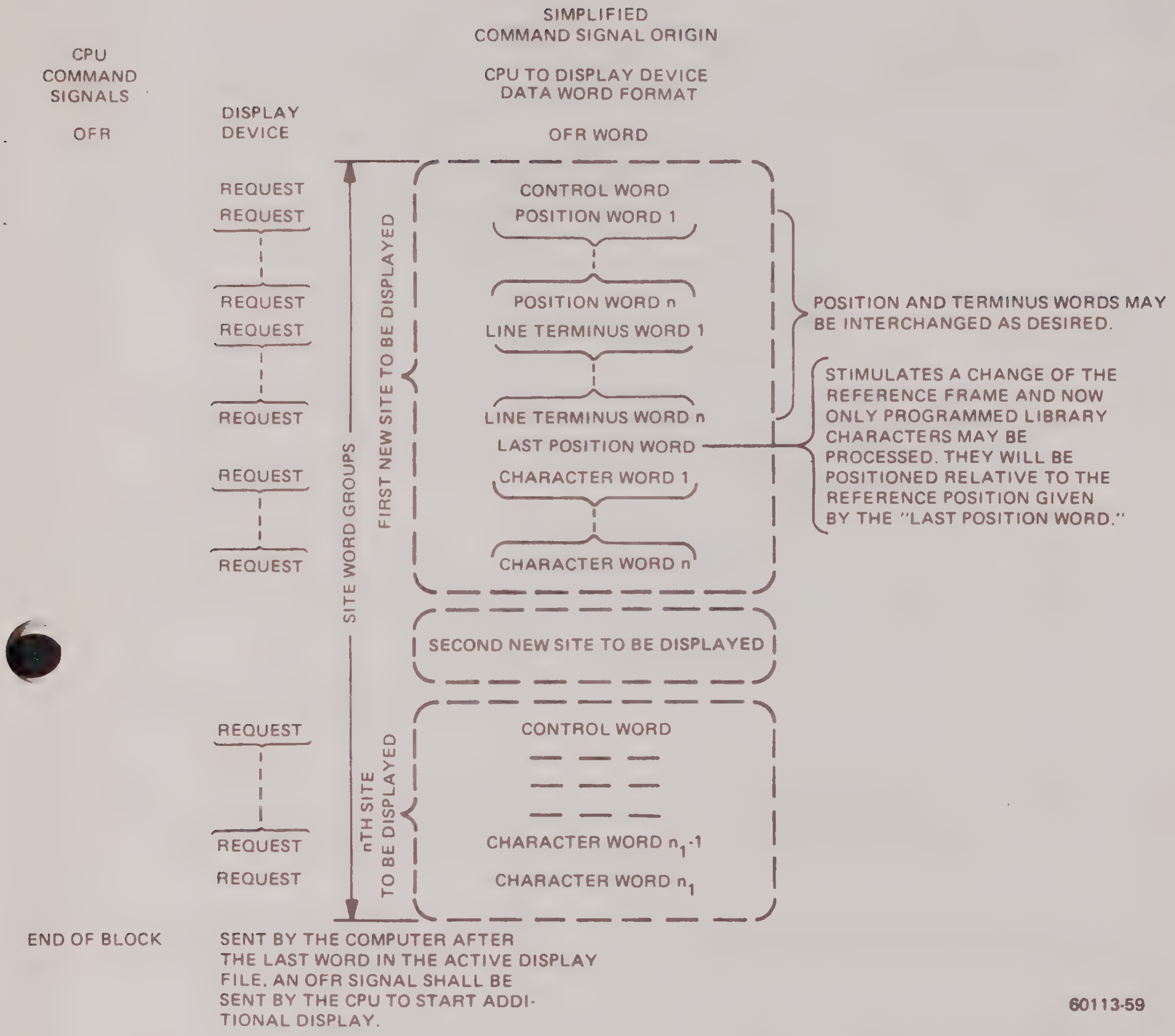

SIMPLIFIED
COMMAND SIGNAL ORIGIN
CPU COMMAND SIGNALS
OFR
DISPLAY DEVICE
CPU TO DISPLAY DEVICE DATA WORD FORMAT
OFR WORD
REQUEST
REQUEST
REQUEST
REQUEST
REQUEST
REQUEST
REQUEST
SITE WORD GROUPS
FIRST NEW SITE TO BE DISPLAYED
CONTROL WORD
POSITION WORD 1
POSITION WORD n
LINE TERMINUS WORD 1
LINE TERMINUS WORD n
LAST POSITION WORD
CHARACTER WORD 1
CHARACTER WORD n
POSITION AND TERMINUS WORDS MAY BE INTERCHANGED AS DESIRED.
STIMULATES A CHANGE OF THE REFERENCE FRAME AND NOW ONLY PROGRAMMED LIBRARY CHARACTERS MAY BE PROCESSED. THEY WILL BE POSITIONED RELATIVE TO THE REFERENCE POSITION GIVEN BY THE "LAST POSITION WORD."
SECOND NEW SITE TO BE DISPLAYED
REQUEST
REQUEST
REQUEST
nTH SITE TO BE DISPLAYED
CONTROL WORD
CHARACTER WORD n_1-1
CHARACTER WORD n_1
END OF BLOCK
SENT BY THE COMPUTER AFTER THE LAST WORD IN THE ACTIVE DISPLAY FILE. AN OFR SIGNAL SHALL BE SENT BY THE CPU TO START ADDITIONAL DISPLAY.
60113-59

Figure B6-24. DPM Data Structures

B7-1. ELP General

The electronic line printer (ELP) provides a hard copy output of various alphanumeric data and special symbols under computer control. The ELP uses non-impact thermal printing to form the required characters (figure B7-1).

B7-2. ELP Capabilities

The ELP can print at the minimum rate of 350 lines per minute or space blank lines at 500 lines per minute. Data storage within the ELP is by single character and printing is by single line. The character set is as shown in figure B7-2.

B7-3. ELP References

ELP Development Specification, EL-CP-00041108

B7-4. ELP-to-Computer Interface

Data transfers between the computer and ELP are performed on an automatic input/output and interrupt basis. Communication is via bytes and words with actual data transfers being accomplished on an 8-bit byte basis (figure B7-3).

B7-5. ELP Command and Control Word(s)

Control of the ELP by the computer is accomplished using two types of command formats which are defined as follows:

a. *ELP OFR Word.* Only the most significant byte of this word is used by the ELP for a loop test. The byte is sent back by the ELP to the computer with no modification. The initial transfer is the result of the computer executing an OFR instruction for the ELP. Figure B7-4 illustrates the OFR word format.

b. *Device Command Byte.* There is only one legal device command, DC 1, which instructs the ELP that the subsequent bytes are ASCII characters to be printed. Figure B7-5 illustrates the DEV command byte format.

B7-6. ELP Status Word(s)

When an ITR command is issued by the computer (ITR instruction for ELP is executed). Device status information is returned to the computer from the ELP, in the form of an ITR word consisting of one 8-bit byte, figures B7-6 and B7-7 define the ITR word/byte contents.

B7-7. ELP Interrupts

The ELP generates an interrupt as a result of receipt of an EOP code or as a result of fault detection. The interrupt sequence causes resetting of the busy bit, transfers of the INTERRUPT byte to the computer, and the return of the ELP to the standby state. The interrupt byte is identical to the ITR status byte in figure B7-6.

B7-8. ELP Data Structures

Transfer of data bytes to the ELP are preceded by a Device command. The data bytes are actually from 1 or N ASCII characters. The ASCII byte format is illustrated in figure B7-8. ASCII command codes contained in the data buffer are honored by the ELP; therefore some caution must be exercised when setting up the buffer.

B7-9. ELP Special Considerations

The ELP responds to format control characters as follows:

a. Performs automatic CR and LF functions after printing the 72nd character in a line.

b. Performs CR and LF functions when the CR character is received.

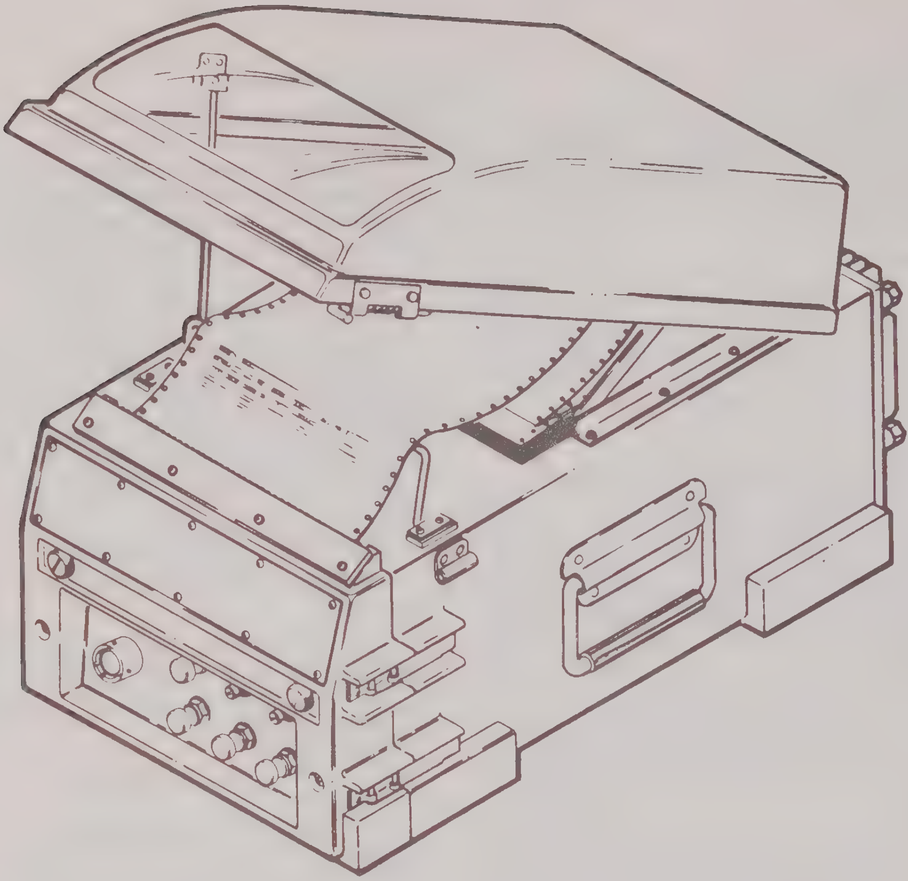
c. Performs an LF function when only the LF character is received.

d. Ignores an LF character following a CR character.

e. If either a CR or LF character appears in a data stream corresponding to the first two character positions after the response given in subparagraph a, it is treated as a NUL.

f. The receipt of a form-feed character causes the stored data to be printed, advances the paper to the next full-form increment, and restores the lefthand margin. A form is defined as that length of paper between perforations in the required fan-fold paper.

Furthermore, the ELP has the means to recognize the vicinity of the form-fold and to skip over the perforations. When using the loop test feature of the ELP, a one-word buffer must be provided to accept the returned data byte. This requires the setup of a keyword and termination word for the device channel prior to executing the OFR instruction.



60113-60

Figure B7-1. Electronic Line Printer

Column→	0	1	2	3	4	5	6	7	R o w ↓
b7 b6 b5	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1	
b4 b3 b2 b1									
0 0 0 0	NUL		SP	0	@	P	@	P	0
0 0 0 1		DC1	!	1	A	Q	A	Q	1
0 0 1 0			"	2	B	R	B	R	2
0 0 1 1			#	3	C	S	C	S	3
0 1 0 0	EOT[1]		$	4	D	T	D	T	4
0 1 0 1		NAK[1]	%	5	E	U	E	U	5
0 1 1 0	ACK[1]		&	6	F	V	F	V	6
0 1 1 1	BEL		(apos)	7	G	W	G	W	7
1 0 0 0			(	8	H	X	H	X	8
1 0 0 1			)	9	I	Y	I	Y	9
1 0 1 0	LF		*	:	J	Z	J	Z	10
1 0 1 1			+	;	K	[	K	[	11
1 1 0 0	FF		,	<	L	\	L	\	12
1 1 0 1	CR		–	=	M	]	M	]	13
1 1 1 0			.	>	N	∧	N	∧	14
1 1 1 1			/	?	O	—	O	—	15

NOTES:

1. Columns 0 and 1 are nondisplay control codes except for

   EOT (⫤)
   ACK (⋈)
   NAK (⊗)

2. The noncoded diamond (◊) symbol is displayed to indicate receipt of an erroneous character.
3. NUL, LF, CR, DC1, BEL, FF and SP are nondisplay codes.
4. Example of code:

P	b7	b6	b5	b4	b3	b2	b1	
1	0	1	0	0	1	0	0	= $
M S B							L S B	

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Figure B7-2. Alphanumeric Display Character Set (64-Character Symbol Subset)

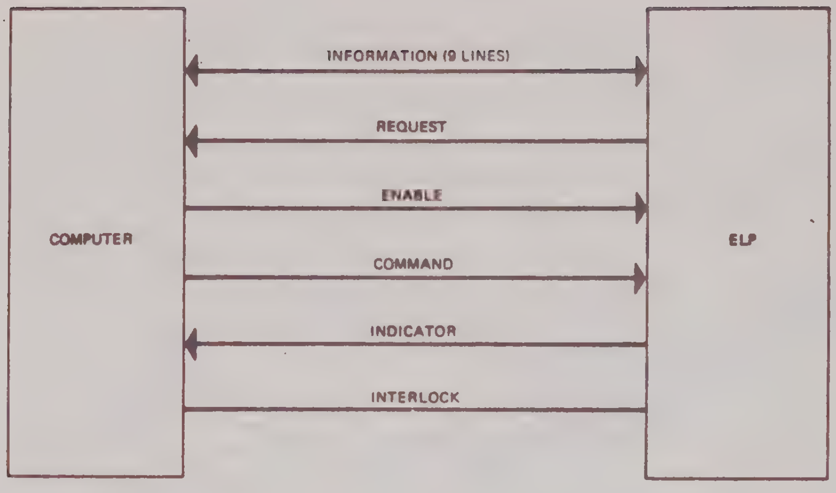
INFORMATION (9 LINES)
REQUEST
ENABLE
COMMAND
INDICATOR
INTERLOCK
COMPUTER
ELP
80113-62

Figure B7-3. ELP-to-Computer Interface

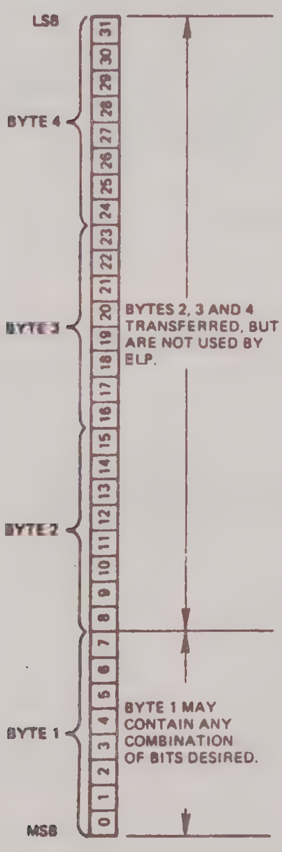
LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
BYTES 2, 3 AND 4 TRANSFERRED, BUT ARE NOT USED BY ELP.
BYTE 1 MAY CONTAIN ANY COMBINATION OF BITS DESIRED.
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Figure B7-4. ELP OFR Word

LSB	7	PARITY (ODD)
	6	"1"
	5	"0"
	4	"0"
	3	"1"
	2	"0"
	1	"0"
MSB	0	"0"

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Figure B7-5. Device Command Byte

LSB	7	"1"
	6	MANUAL TEST IN PROCESS
	5	PRINTER FAULT
	4	PARITY ERROR
	3	PARITY ERROR, LP
	2	13 FORMS OR LESS OF PAPER REMAINING
	1	ELP BUSY
MSB	0	NOT ASSIGNED

NOTE: THIS BYTE WILL BE INPUT TO THE COMPUTER WITHOUT PARITY GENERATION ON INFORMATION LINE P.

70061-169

Figure B7-6. ELP ITR/Interrupt Status Byte

Bit	Description
0	Spare (not assigned).
1	Busy. The ELP sets this bit = 1 when the ELP is busy (unable to accept a DEV or OFR command). This bit is set by the ELPs acknowledgement of receipt of a DEV or OFR command. This bit shall be reset (bit = 0) by the ELP initiation of an interrupt sequence, either after an EOB command or an error/fault interrupt, or by a Device Stop or Master Reset command.
2	780 lines or less of paper remaining. This bit shall be reset by refilling the paper supply.
3	LP parity error. (This bit shall be true when the ELP detects a parity error during automatic I/O operation).
4	Parity error. The ELP is sent an interrupt sequence and transmit the status byte to the computer when a parity error in the data character is detected. The ELP implementation shall provide for the following: a. The ELP logic shall be such as to detect a parity error in a received data byte, and transmit the interrupt sequence, prior to requesting the next data byte. b. In the A configuration there shall be no more than one character at a time in the ELP dynamic buffer. c. An EOB command shall be ignored if a parity error is detected. d. Before initiating the interrupt sequence, the ELP shall clear the dynamic buffer and perform an LF. This bit shall be reset by receipt of a DEV or OFR command.
5	Printer fault. This bit shall be set when there is a printer fault.
6	Manual test in process. This bit shall be set when the ELP internal test function is in process. The bit shall be reset upon completion of the test.
7	"1". This bit shall be a logical one.

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Figure B7-7. ELP ITR/Interrupt Status Bits

LSB	7	ASCII b1
	6	ASCII b2
	5	ASCII b3
	4	ASCII b4
	3	ASCII b5
	2	ASCII b6
	1	ASCII b7
MSB	0	PARITY (ODD)

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Figure B7-8. ELP ASCII Data Byte

Section VIII. ELECTRONIC TACTICAL DISPLAY

B8-1. ETD General

The electronic tactical display (ETD) converts computer-stored digital data into a visual real-time CRT presentation under computer control (figure B8-1). The presentation capability of the display covers the following:

a. Lines, grids, and circular and irregularly shaped areas with associated alphanumerics.

b. Special symbols and alerts as required by the particular application.

c. A test pattern via the computer to verify ETD operability.

The display presentation may be modified by the ETD operator, using category selection, display offset, and scale selection. Individual symbols also may be "hooked" via the light pen. Additionally provided is the capability to add an alphanumeric keyboard to the ETD, thereby allowing considerable flexibility at the man/machine interface.

B8-2. ETD Capabilities

The ETD can generate approximately 100 different types of symbols and alphanumerics for display on its 16-inch circular CRT. Individual element positioning is done in X and Y coordinates with an allowed error of ±1/1024 in each axis. The symbols (figures B8-2 and B8-3) and alphanumerics (figure B8-4) are generated by the ETD, internally. However, the ETD has no data buffer and must be refreshed continuously at a nominal 30 Hz rate. Figure B8-5 illustrates a typical ETD presentation.

B8-3. ETD References

ETD Development Specification, EL-CP-00041104

ETD Technical Manual, TM 11-7440-250-35

Message and Codes Standards Specification, EL-SS-0004-R-3

B8-4. ETD-to-Computer Interface

Data transfer between the computer and ETD is performed on an automatic input/output basis. Communication is on a 32-bit word basis with actual data transfers being accomplished via 8-bit bytes using nine information lines (8 data and 1 parity) and four additional control lines (figure B8-6).

B8-5. ETD Command and Control Word(s)

Control of the ETD presentation by the computer is accomplished, using four types of command words.

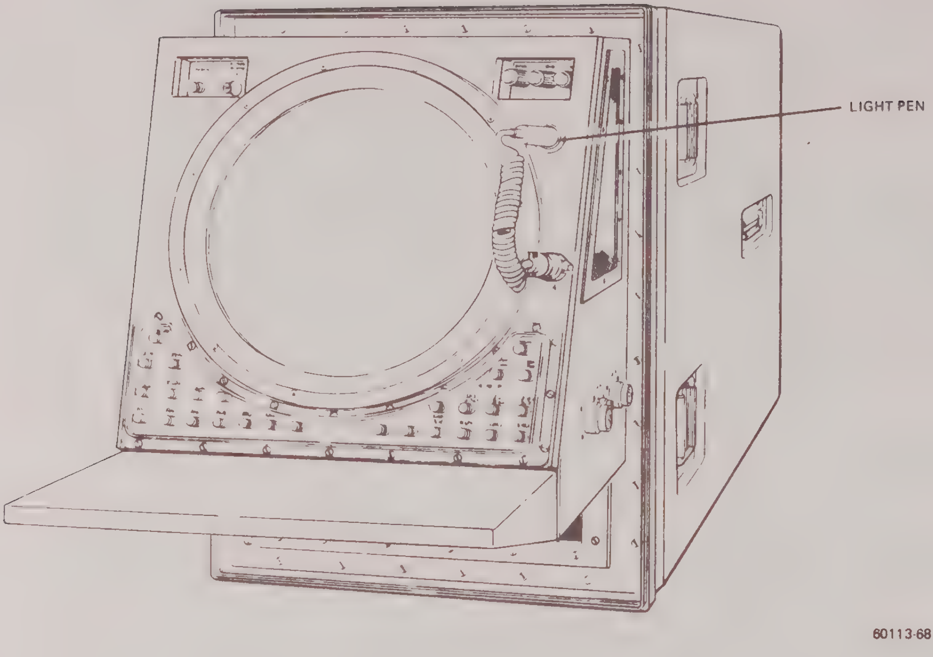


Figure B8-1. Electronic Tactical Display

Their format and purpose are defined in the following paragraphs and figures.

a. *OFR Word (figures B8-7 and B8-8).* An OFR command is transferred to the ETD, once at the start of each CPU-controlled refresh cycle (OFR instruction for ETD is executed).

b. *Control Word (figures B8-9 and B8-10).* A control word is sent to the ETD for each of the three site/word groups.

c. *Position Word (figures B8-11 and B8-12).* One or more position words are sent to the ETD within each site/word group. The actual number varies with respect to the complexity of the presentation. This word format defines a position on the CRT, relative to the basic reference point of the ETD, which is the lower lefthand corner of the display.

d. *Character Word (figures B8-13 and B8-14).* Character words are used to define which characters or symbols are to be displayed. Four characters/symbols may be defined in one word along with the row-column information, locating the first element within the character field matrix, as shown in figure B8-15.

B8-6. ETD Status Word(s)

Device status information is returned to the computer from the ETD in the form of ITR words 1, 2 or 3 when an ITR command is issued by the computer (ITR instruction for ETD is executed). The format and purpose of these ITR words are defined in the following paragraphs and figures.

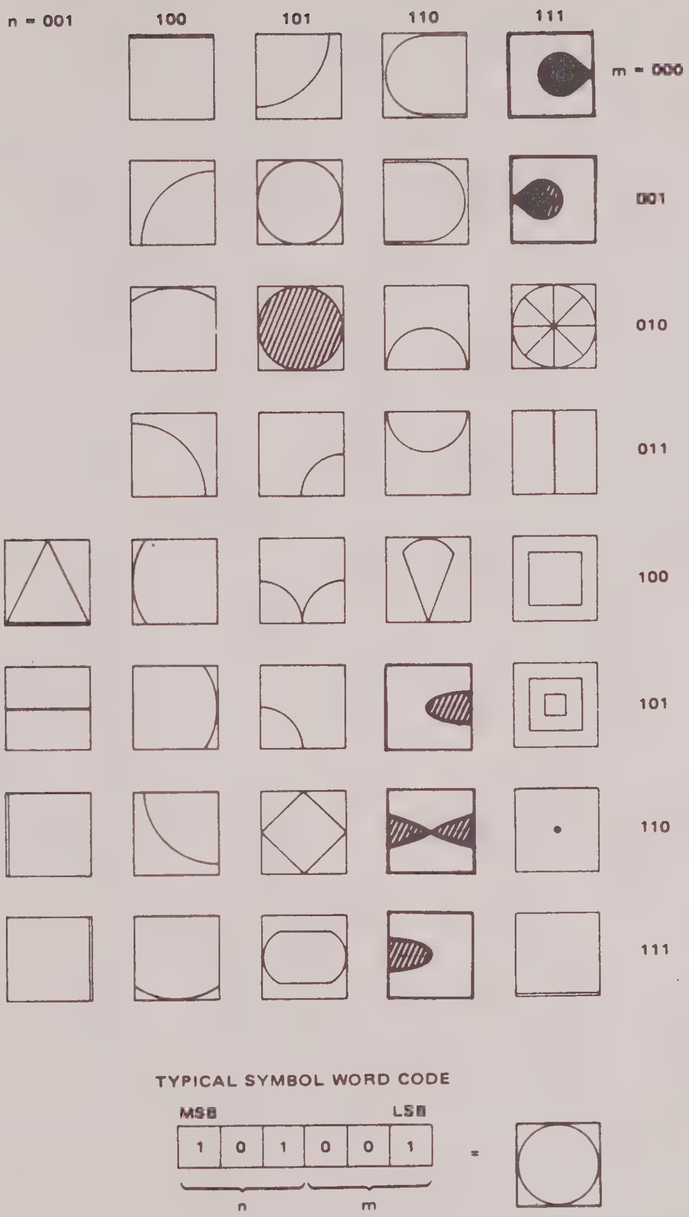
a. *ITR1 Word (figures B8-16 and B8-17).* Contains switch code data reflecting the status of the ETD front panel switches.

b. *ITR2 Word (figures B8-18 and B8-19).* Contains alphanumeric keyboard code data.

c. *ITR3 Word (figures B8-20 and B8-21).* Contains diagnostic data resulting from diagnostic register code as defined in a previous OFR.

B8-7. ETD Interrupts

The only ETD-generated interrupt results from pressing the light pen pushbutton (see Special Considerations, B8-9). There is no interrupt data byte associated with the ETD interrupt sequence.


n = 001
100
101
110
111
m = 000
001
010
011
100
101
110
111
TYPICAL SYMBOL WORD CODE
MSB
LSB
1
0
1
0
0
1
=
n
m

CODE 000000 = BLANK (NO SYMBOL)

NOTE: BOX AROUND SYMBOL IS
NOT PART OF SYMBOL. IT IS SHOWN
HERE FOR REFERENCE ONLY.

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Figure B8-2. ETD Symbol Library

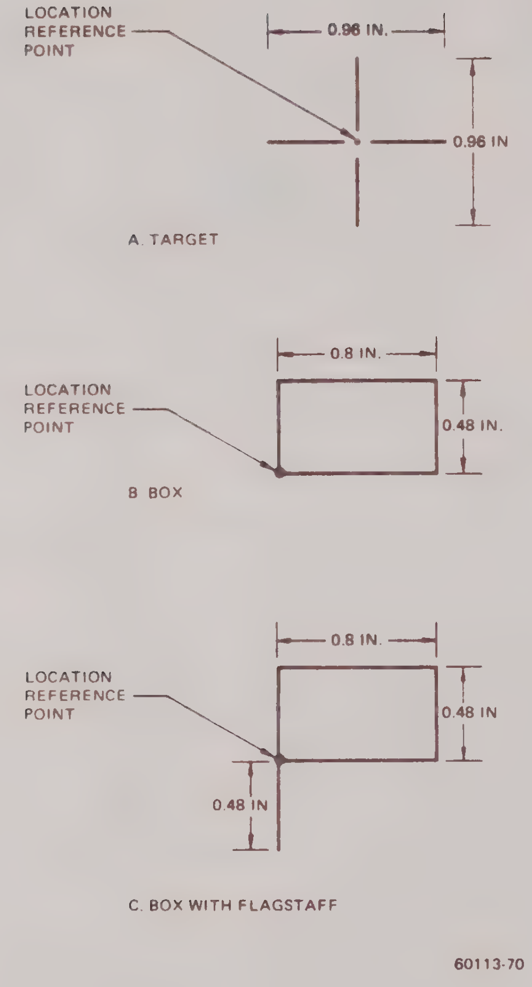
LOCATION REFERENCE POINT
0.96 IN.
0.96 IN
A. TARGET
0.8 IN.
LOCATION REFERENCE POINT
0.48 IN.
B BOX
0.8 IN.
LOCATION REFERENCE POINT
0.48 IN
0.48 IN
C. BOX WITH FLAGSTAFF
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Figure B8-3. ETD Special Symbols

COLUMN →	0	1	2	3	4	5	6	7	ROW ↓
b7 b5			0 0	0 1	1 0	1 1			
b4 b3 b2 b1									
0 0 0 0			SP	0	@	P			0
0 0 0 1			!	1	A	Q			1
0 0 1 0			"	2	B	R			2
0 0 1 1			#	3	C	S			3
0 1 0 0			$	4	D	T			4
0 1 0 1			%	5	E	U			5
0 1 1 0			&	6	F	V			6
0 1 1 1			' (APOS)	7	G	W			7
1 0 0 0			(	8	H	X			8
1 0 0 1			)	9	I	Y			9
1 0 1 0			*		J	Z			10
1 0 1 1			+	;	K	[			11
1 1 0 0			,	<	L	\			12
1 1 0 1			–	=	M	]			13
1 1 1 0				>	N	^			14
1 1 1 1			/	?	O	_			15

EXAMPLE OF A TYPICAL ALPHANUMERIC CHARACTER CODE:

b7	b6	b4	b3	b2	b1	
0	0	0	1	0	0	= $
MSB					LSB	

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Figure B8-4. Alphanumeric Character Set

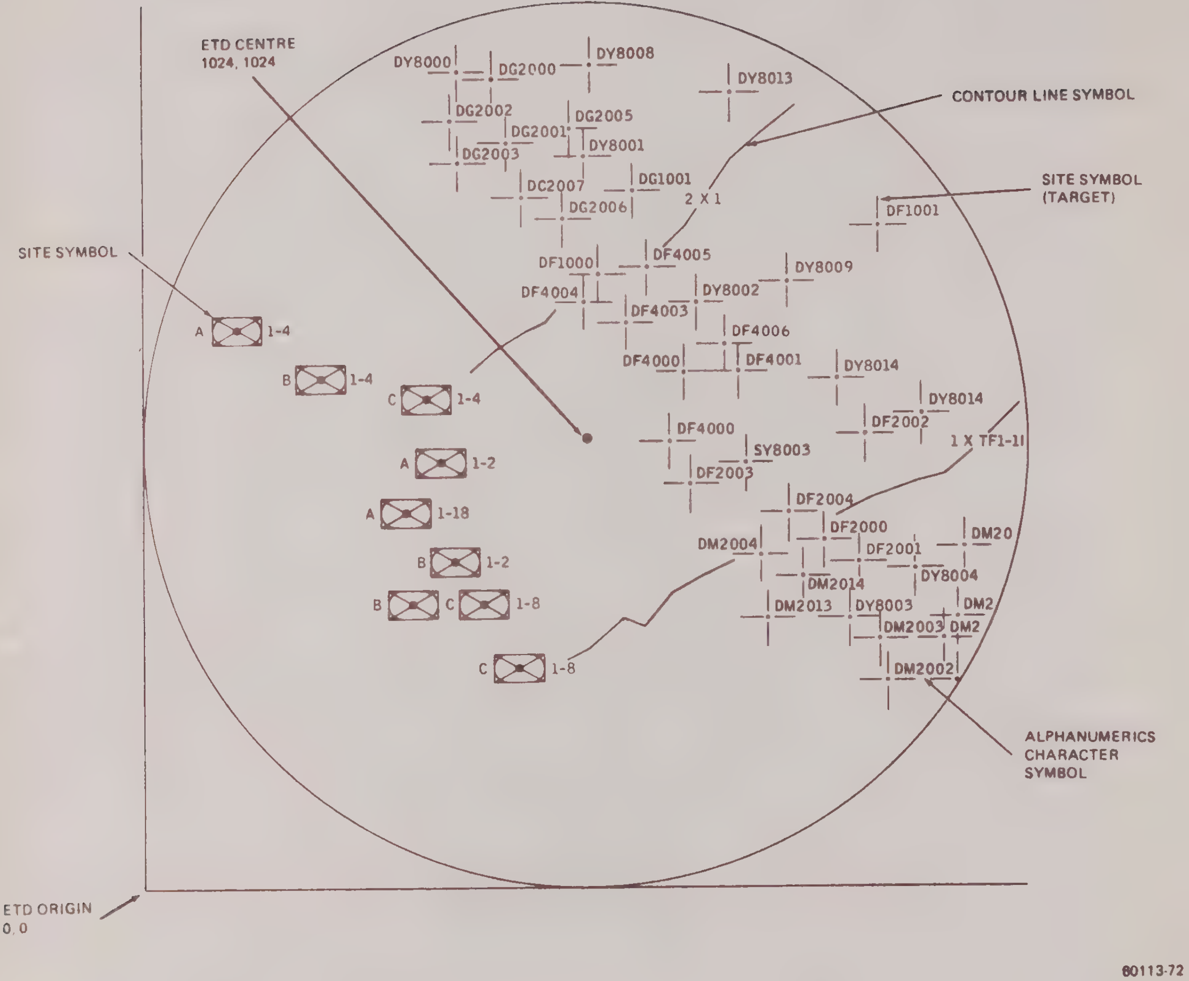

ETD CENTRE
1024, 1024
DY8000
DG2000
DY8008
DY8013
CONTOUR LINE SYMBOL
DG2002
DG2005
DG2001
DY8001
DG2003
DC2007
DG1001
DG2006
2 X 1
SITE SYMBOL
(TARGET)
DF1001
SITE SYMBOL
DF1000
DF4005
DY8009
DF4004
DY8002
DF4003
A
1-4
DF4006
B
1-4
DF4000
DF4001
DY8014
C
1-4
DY8014
DF2002
DF4000
1 X TF1-11
SY8003
A
1-2
DF2003
A
1-18
DF2004
DF2000
DM20
DM2004
DF2001
B
1-2
DY8004
DM2014
B
C
1-8
DM2013
DY8003
DM2
DM2003
DM2
C
1-8
DM2002
ALPHANUMERICS
CHARACTER
SYMBOL
ETD ORIGIN
0, 0
80113-72

Figure B8-5. ETD Typical Symbology Display

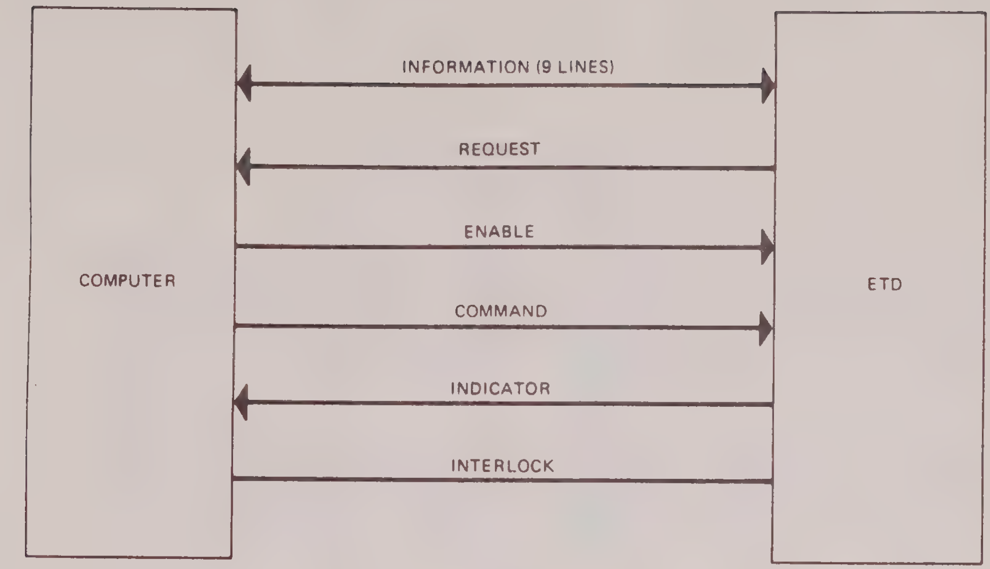


Figure B8-6. ETD-to-Computer Interface

B8-8. ETD Data Structures

In the current implementation there are three data classifications that comprise site/word groups. These are defined as follows and illustrated in figure B8-22.

a. *Situation/Line Data.* Situation/line data consists of one control word, one or more position words, and one or more character words in that order repeated sequentially. This word group is used to generate site information (box, box with flagstaff, target site) and graphic information (fire lines, etc.) along with symbolic and alphanumeric information.

b. *Offset Point Data.* Offset point data consists of one control word with the offset points bit set and at least one position word. Offset point data allows the generation of offset points on the display.

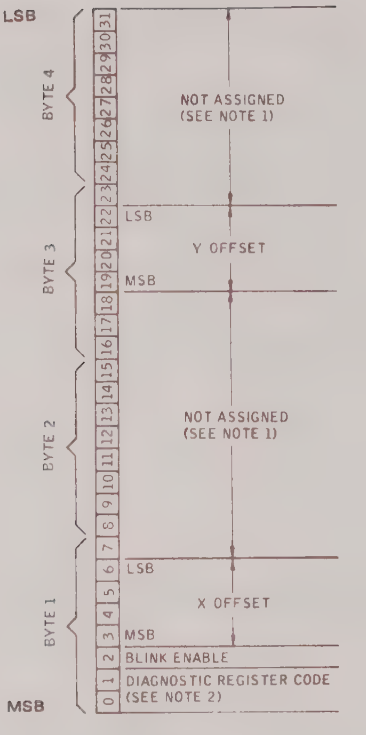
c. *Tabular Data.* Tabular data consists of a control word, a position word, and a series of character words. The information in the character word is displayed in words on a predetermined CRT area.

It should be noted that the data structures are only combinations of the previously defined command words; other combination than those described may be allowable, depending on the application.

B8-9. ETD Special Considerations

The interrupt caused by depressing the light pen pushbutton marks the point in time when the ETD scan has reached the position of the light pen. It is up to the program to determine what this position is and take whatever actions may be required.

Since the ETD requires continuous refreshing, care must be exercised in defining data buffer limits and device channel assignments. Display flicker becomes pronounced if the refresh rate drops too low due to excess data, channel loading, or any other time limitations that may appear.


LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
NOT ASSIGNED
(SEE NOTE 1)
LSB
Y OFFSET
MSB
NOT ASSIGNED
(SEE NOTE 1)
LSB
X OFFSET
MSB
BLINK ENABLE
DIAGNOSTIC REGISTER CODE
(SEE NOTE 2)

NOTES:

1. NOT ASSIGNED FIELDS MAY BE "1" OR "0".
2. THE DIAGNOSTIC REGISTER CODE IS AS FOLLOWS·

BIT 0	BIT 1	REGISTER NO.
0	0	1
0	1	2
1	0	3
1	1	4

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Figure B8-7. Computer to ETD, OFR Word Format

Bit	Description
0, 1	Diagnostic register code. This field contains a bit code defining the contents of the ETD diagnostic register field contained in ITR3 word resulting from the third ITR signal. The diagnostic register code is under the control of the diagnostic program related to the ETD operational status check.
2	Blink enable. This bit is set equal to ONE for a series of consecutive OFR data words determined as a function of the ETD refresh rate. An ETD refresh rate of 30 Hz requires that the blink enable bit be true for 15 consecutive OFRs and false for 15 OFRs to produce a blink rate of approximately 1 Hz.
3 through 6	X offset. This field is equal to the four most significant bits of the 11-bit X-position data contained in the position word corresponding to the selected console offset point.
7 through 18	Not assigned.
19 through 22	Y offset. This field is equal to the four most-significant-bits of the 11-bit Y-position data contained in the position word corresponding to the selected console offset point.
23 through 31	Not assigned.

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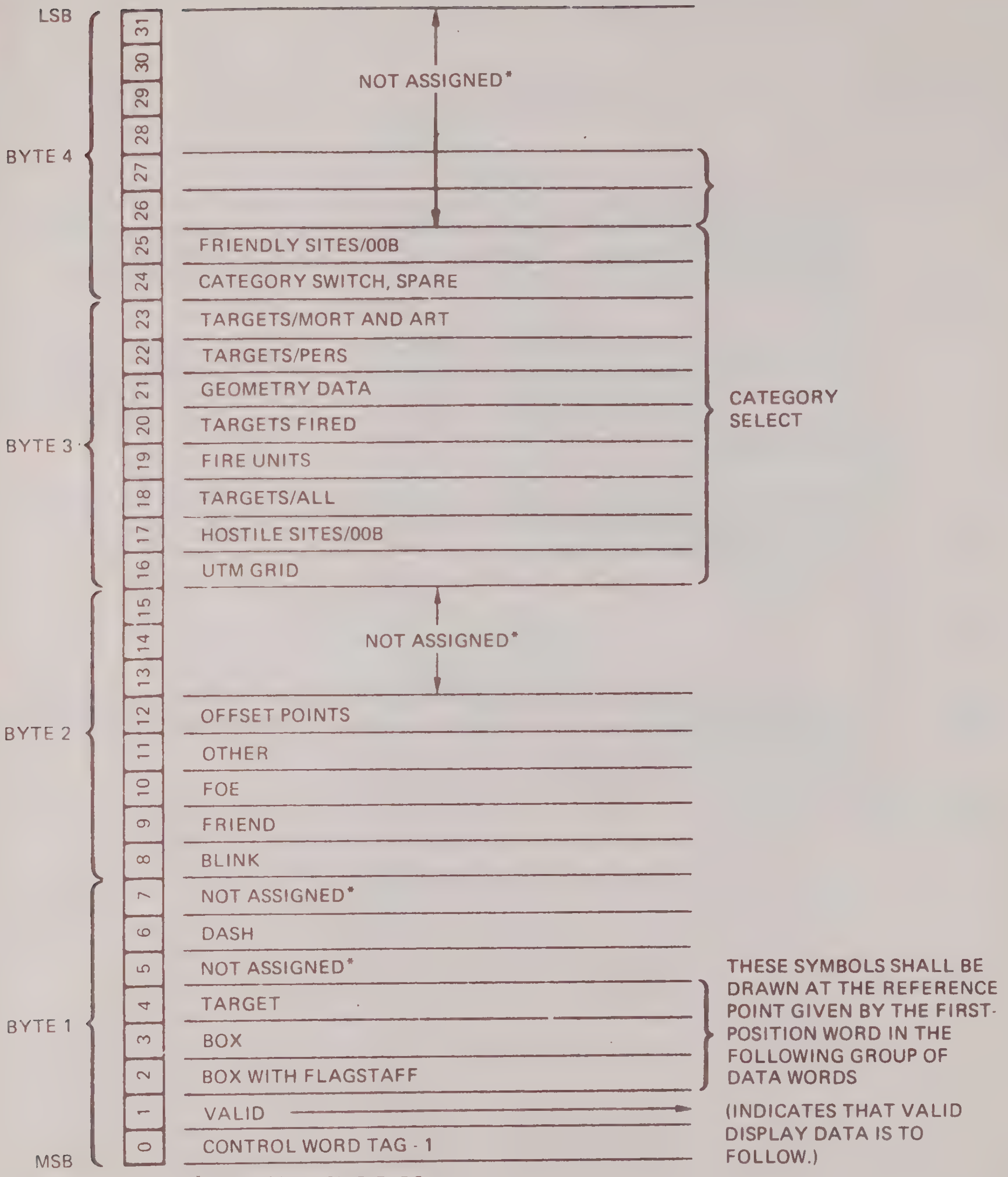
Figure B8-8. OFR Word Content and Usage


LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
NOT ASSIGNED*
FRIENDLY SITES/00B
CATEGORY SWITCH, SPARE
TARGETS/MORT AND ART
TARGETS/PERS
GEOMETRY DATA
TARGETS FIRED
FIRE UNITS
TARGETS/ALL
HOSTILE SITES/00B
UTM GRID
CATEGORY SELECT
NOT ASSIGNED*
OFFSET POINTS
OTHER
FOE
FRIEND
BLINK
NOT ASSIGNED*
DASH
NOT ASSIGNED*
TARGET
BOX
BOX WITH FLAGSTAFF
THESE SYMBOLS SHALL BE DRAWN AT THE REFERENCE POINT GIVEN BY THE FIRST-POSITION WORD IN THE FOLLOWING GROUP OF DATA WORDS
VALID
(INDICATES THAT VALID DISPLAY DATA IS TO FOLLOW.)
CONTROL WORD TAG - 1

*NOT ASSIGNED FIELDS
MAY BE "1 OR 0"

60113-76

Figure B8-9. Computer to ETD Control Word Format

Bit	Description
0	Control word tag. This tag, when equal to ONE, is used to uniquely identify the message as a control word.
1	Valid. This bit, when equal to ONE, indicates that display data is to follow the control word. A valid bit equal to ZERO causes the ETD to reject the data words associated with the control word and it continues requesting, through the display output file, until a valid control word is received. The valid bit is set equal to ZERO in response to an ETD operator's hook and suppress action (refer to DTM 11-7440-241-12).
2	Box with flagstaff. This bit is used by the ETD to activate fixed logic circuitry for generation of the box flagstaff symbology.
3	Box. This bit is used by the ETD to activate fixed logic circuitry for generation of the box symbology.
4	Target. This bit is used by the ETD to activate fixed logic circuitry for generation of the target site symbology.
6	Dash. This bit is used within the ETD to display the sides of the box flagstaff symbology, as broken lines, by alternately blanking and unblanking the Z-axis.
5, 7	Not assigned.
8	Blink. This bit is used by the ETD in conjunction with the status of the blink enable bit in OFR data word to display symbology at an approximate one Hz blinking rate.
9	Friend. This bit indicates to the ETD that the data words to follow pertain to a symbology set which is in the general classification of friendly.
10	Foe. This bit indicates to the ETD that the data words to follow pertain to a symbology set which is in the general classification of hostile.
11	Other. This bit indicates to the ETD that the data words to follow pertain to a symbology set which is in the general classification of other than target site, friend, or foe. Specifically, the other bit is a ONE when either tabular data or contiguous line information is to follow the control word. The target, friend, foe, and other bits is mutually exclusive.
12	Offset Points. This bit shall be true in one, and only one, control word of the display output file. This bit, when true, will indicate to the ETD that a set of up to nine position words is to follow the control word. These position words will be referenced to the console grid and will represent the array of displayable console offset points.

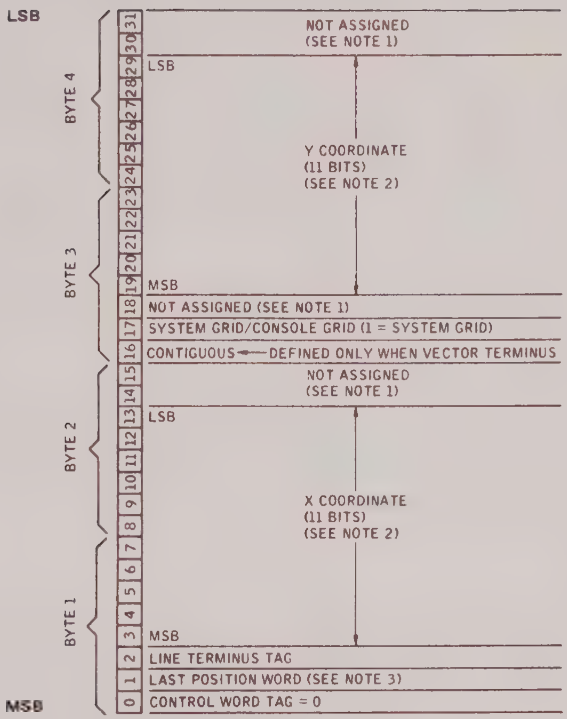
60113-77-1

Figure B8-10. Control Word Content and Usage (Sheet 1 of 2)

Bit	Description
13 through 15	Not Assigned.
16 through 25	Category Select. This field will contain 10 bits which are uniquely related, on a one-to-one basis, to a set of 10 DATA SELECT lighted pushbutton switches on the ETD front panel. The bit pattern in the data select field of the control word will classify the contents of the data words to follow, and will be used by the ETD to determine displayability upon comparison with the corresponding set of DATA SELECT switches. If there is no match of any category select switch bit with its corresponding data select switch, the ETD continues requesting through the computer-generated display output file, until a valid control word is received with a successful comparison with at least one of the categories.
26 through 31	Not Assigned.

60113-77-2

Figure B8-10. Control Word Content and Usage (Sheet 2 of 2)


LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31 30
NOT ASSIGNED (SEE NOTE 1)
29 28 27 26 25 24 23 22 21 20 19
LSB
Y COORDINATE (11 BITS) (SEE NOTE 2)
MSB
18
NOT ASSIGNED (SEE NOTE 1)
17
SYSTEM GRID/CONSOLE GRID (1 = SYSTEM GRID)
16
CONTIGUOUS ← DEFINED ONLY WHEN VECTOR TERMINUS
15 14
NOT ASSIGNED (SEE NOTE 1)
13 12 11 10 9 8 7 6 5 4 3
LSB
X COORDINATE (11 BITS) (SEE NOTE 2)
MSB
2
LINE TERMINUS TAG
1
LAST POSITION WORD (SEE NOTE 3)
0
CONTROL WORD TAG = 0

NOTES:

1. NOT ASSIGNED FIELDS MAY BE "1" OR "0".
2. 0, 0 = LOWER LEFT CORNER OF DISPLAY.
3. THIS BIT INDICATES THE LAST IN A SEQUENCE OF POSITION WORDS AND THAT THE FOLLOWING WORDS WILL BE SYMBOL WORDS, FOLLOWED BY AN IDENTIFIED CONTROL WORD.

70061-171

Figure B8-11. Computer to ETD, Position Word Format

Bit	Description
0	Control word tag. This tag, when equal to ZERO, is used to identify the message as a noncontrol word. All data words received by the ETD after a control word are interpreted as position words until a word containing the last position word bit equal to ONE is acknowledged.
1	Last position word. This bit, when equal to ONE, indicates the end of a position word set following a control word. Because no bits are used to uniquely distinguish position words from character words, a strict sequence of word organization in the display output file is adhered to; i.e., a single control word followed by m position words, followed by n character words, where m = 1 to 100 and n = 0 to 100.
2	Line terminus tag. This tag is set equal to ONE in the position word which contains the positional information corresponding to the terminus for the last line of a contiguous line set.
3 through 13	X-coordinate. This field consists of 11 bits containing the X-value of a position defined within the system grid. The MSB of the X-coordinate is a ZERO in all X-coordinate fields defining points to the left of center in the X-axis, and a ONE in all X-coordinate fields defining points to the right of center in the X-axis.
14, 15	Not assigned.
16	Contiguous. This bit is a ONE in all position words which represent the terminus of a line in a contiguous line set. Upon detection of the first position word containing a contiguous bit equal to ONE, the ETD causes a line to be drawn to that point using the position received in the previous position word as the origin for the first contiguous line. This process is repeated for the entire set of contiguous lines until a position word is received which contains both a contiguous bit and a line terminus tag equal to ONE.
17	System grid/console grid. This bit is set to a ONE when the positional information contained in the position word is referenced to the center of the system grid. When equal to ZERO, the ETD interprets the positional X-Y coordinate information as being referenced to the center of the console grid, and bypasses the logic networks required to condition positional data with the selected console offset and expansion scale.
18	Not assigned.

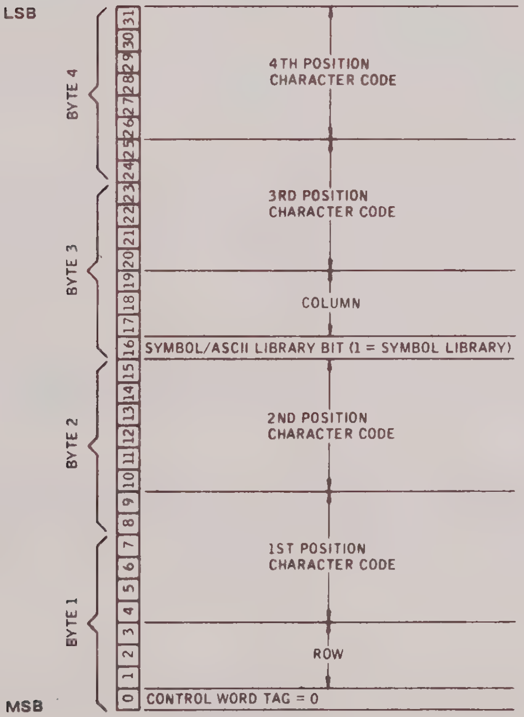
60113-79-1

Figure B8-12. Position Word Content and Usage (Sheet 1 of 2)

Bit	Description
19 through 29	Y-coordinate. This field consists of 11 bits containing the Y-value of a position defined within the system grid. The MSB of the Y-coordinate is a ZERO in all Y-coordinate fields defining points below center in the Y-axis, and a ONE in all Y-coordinate fields defining points above center in Y-axis.
30, 31	Not assigned.

60113-79-2

Figure B8-12. Position Word Content and Usage (Sheet 2 of 2)


LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
29
30
31
4TH POSITION CHARACTER CODE
3RD POSITION CHARACTER CODE
COLUMN
SYMBOL/ASCII LIBRARY BIT (1 = SYMBOL LIBRARY)
2ND POSITION CHARACTER CODE
1ST POSITION CHARACTER CODE
ROW
CONTROL WORD TAG = 0

70061-172

Figure B8-13. Computer to ETD, Character Word Format

Bit	Description
0	Control word tag. This tag, when equal to ZERO, is used to identify the message as a noncontrol word. The first noncontrol word transmitted to the ETD after a position word containing a last position word-bit equal to ONE is interpreted as a character word as will all following words until a new control word is received.
1 through 3	Row. The row address is a 3-bit field defining one of seven display rows in the character field matrix. The row code is used to define the vertical location of characters displayed in the character field matrix.
4 through 9	Character code, first position. This field contains a 6-bit symbol/ character code pertinent to the information to be displayed in the first cell of each four-cell packet contained in the character field matrix.
10 through 15	Character code, second position. This field contains a 6-bit symbol/ character code pertinent to the information displayed in second cell of each four-cell packet contained in the character field matrix.
16	Symbol/ASCII library bit. This bit, when equal to ONE, indicates that the four, 6-bit character codes pertain to the symbol library. When equal to ZERO, this bit causes the six, 6-bit character codes to be interpreted as ASCII characters.
17 through 19	Column. The column address is a 3-bit field defining the lower left-hand corner of one of five display columns in the character field matrix. Each column contains four character cells. The column code is used to define the horizontal location of characters to be displayed in a line or row of the character field matrix.
20 through 25	Character code, third position. This field contains a 6-bit symbol/ character code pertinent to the information displayed in the third cell of each four-cell packet contained in the character field matrix.
26 through 31	Character code, fourth position. This field contains a 6-bit symbol/ character code pertinent to the information to be displayed in the fourth cell of each fourth-cell packet contained in the character field matrix.

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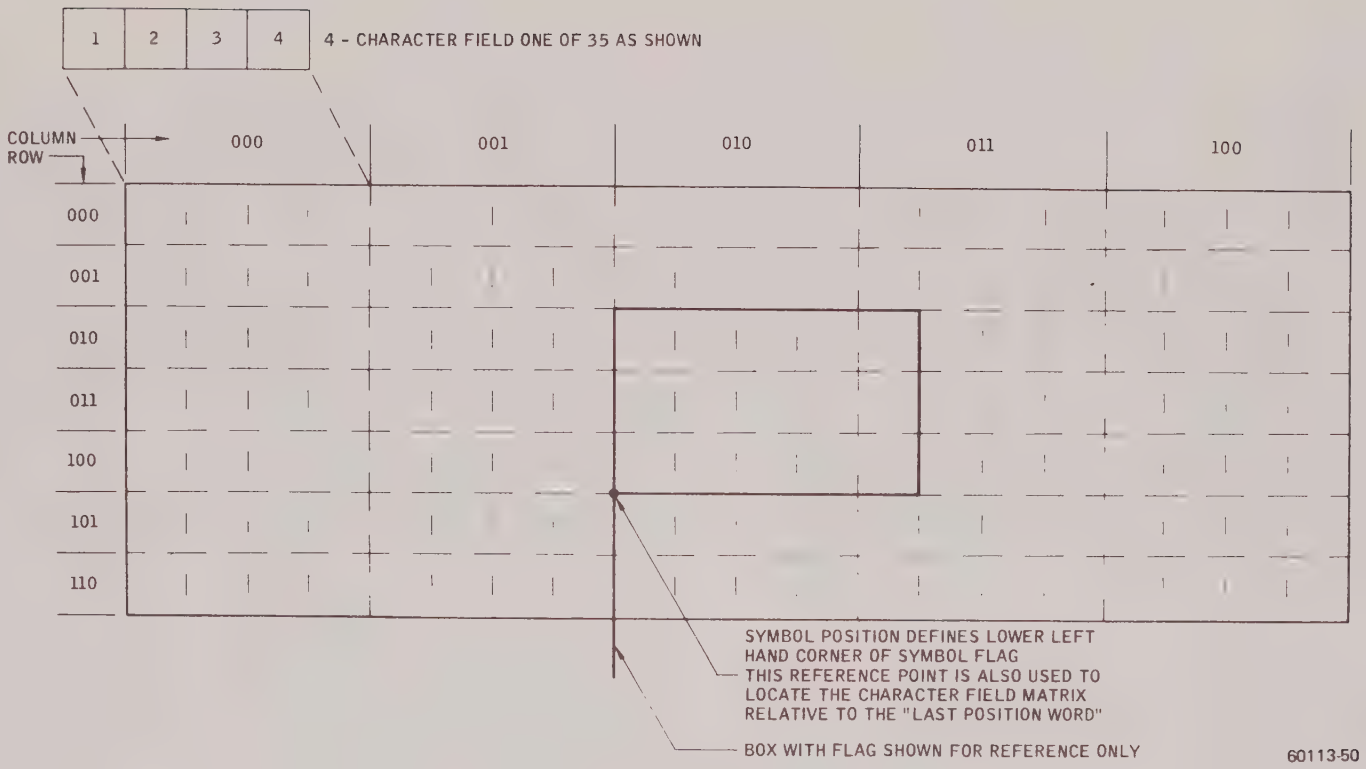
Figure B8-14. ETD Character Word Content and Usage


1
2
3
4
COLUMN
ROW
000
001
010
011
100
000
001
010
011
100
101
110

4 - CHARACTER FIELD ONE OF 35 AS SHOWN

SYMBOL POSITION DEFINES LOWER LEFT HAND CORNER OF SYMBOL FLAG
THIS REFERENCE POINT IS ALSO USED TO LOCATE THE CHARACTER FIELD MATRIX RELATIVE TO THE "LAST POSITION WORD"

BOX WITH FLAG SHOWN FOR REFERENCE ONLY

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Figure B8-15 Character Matrix

LSB	BYTE 4	31	PARITY ERROR	
		30	TEST	
		29	LIGHT PEN	
		28	LAST WORD/NEXT TO LAST WORD (1 = LAST WORD)	
		27	SPARE	
		26	DELETE	
		25	FRIENDLY SITES/OOB	CATEGORY SELECT
		24	SPARE	
	BYTE 3	23	TARGETS/MORT & ART	
		22	TARGETS/PERS	
		21	GEOMETRY DATA	
		20	TARGETS FIRED	
		19	FIRE UNITS	
		18	TARGETS/ALL	
		17	HOSTILE SITES/OOB	
		16	UTM GRID	
	BYTE 2	15	ITR1 CODE 1	
		14	ITR1 CODE 0	
		13	SUPPRESS TARGETS	
		12	DPM DISPLAY	
		11	SHOW TARGET DATA	
		10	RECALL TARGETS	
		9	ACK TARGETS	
		8	ABBR SYMBOLS	
	BYTE 1	7	OFFSET	
		6	OFFSET POINTS	
		5	SPARE	
		4	X4	DISPLAY SCALE
		3	X2	
		2	X1	
		1	CHARACTER ID**	
MSB		0		

*NOT ASSIGNED FIELDS MAY BE "1" OR "0"

**CHARACTER ID CODE IS AS FOLLOWS

BIT 0	BIT 1	CHARACTER NO.
0	0	4
0	1	1
1	0	2
1	1	3

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Figure B8-16. ETD-to-Computer (ITR Format No. 1) Switch Code Format

Bit	Description
0, 1	Character ID. This code shall consist of two bits used to uniquely identify the character, in a packet of four received in a character word, being hooked via the light pen in a character field matrix.
2	X1. This bit shall indicate selection of the X1 display expansion scale.
3	X2. This bit shall indicate selection of the X2 display expansion scale.
4	X4. This bit shall indicate selection of the X4 display expansion scale.
5	Spare.
6	Offset Points. This bit shall indicate that the ETD has selected offset points for display. A pattern of up to nine offset points, with one located at the center of the ETD console grid and the others separated from this portion by a one-half radius in each axis, shall be displayed.
7	Offset. This bit shall be posted when the ETD is hooked to one of the offset points and new offset information is being entered into the computer. The hooked offset points shall be interpreted by the computer as the new display center at the ETD Console.
8	ABBR Symbols. This bit shall be posted upon activation of the ABBR SYMBOLS switch and used by the ETD operator to reduce the clutter of a display. Activation of the ABBR SYMBOLS switch, when its switchcap is not illuminated, shall cause the switchcap to be illuminated and the display on the ETD console to be modified, in conjunction with the corresponding control word, as follows. If either the Friend, Foe, or Target bits of the control word are set, all alphanumeric data shall be inhibited from the display, friendly symbols shall be changed to simple box symbols, enemy symbols shall be changed to simple double-box symbols, and site tick marks shall be changed to dots. The display of simplified symbology in response to activation of the ABBR SYMBOLS switch shall be accomplished by fixed logic in the ETD. All normal computer-generated data in each control word packet, other than the first position word locating the target symbology, shall be ignored. The ETD shall then synthesize, and transmit to its character generator, the appropriate codes for the simplified symbology per the occurrence of either the friend, foe or target site bit in the associated computer-generated control word. If the "other" bit of the control word is set, indicating tabular data, offset points, or contiguous lines data is to follow, then all position words are processed normally while the character words are inhibited from display. Thus, tabular data or alphanumerics associated with the contiguous lines shall not be displayed. Offset Points and the contiguous lines themselves shall be displayed.

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Figure B8-17. ITR1 Word Content and Usage (Sheet 1 of 3)

Bit	Description
	Should none of the four descriptive, mutually exclusive bits (friend, foe, target, or other) in the control word be set, the status of the ABBR SYMBOLS switch shall be ignored for that particular control word data packet. Thus, a programmable "force" is provided whereby certain critical data can still be displayed in normal fashion overriding the ABBR SYMBOLS switch.
9	Ack Targets. This bit shall be posted in response to momentary activation of the ACK (acknowledge) pushbutton switch located on the ETD front panel. This switch shall be used in conjunction with the light pen to acknowledge the receipt of a "blinking" new target. Activation, when hooked, shall cause the target symbol to stop blinking. This shall be accomplished by the computer software setting the blink bit in the appropriate control word equal to ZERO.
10	Recall Targets. This bit shall enable the display of all previously suppressed targets. This action shall be accomplished by the computer software restoring the valid bit in the control word association with each suppressed target.
11	Show Target Data. This bit shall cause a read-out of amplifying data associated with a hooked target to be displayed on the "fixed-size show data" area of the ETD console.
12	DPM Display. This bit shall be posted in response to activation of the DPM Display Momentary Pushbutton switch on the ETD front panel. Activation of this function shall cause hooked data to be displayed on the DPM as directed by the DPS. This function does not apply to geometry data.
13	Suppress Targets. This bit shall be posted in response to activation of the SUPPRESS TARGETS pushbutton on the ETD front panel. Activation of the suppress function when hooked, shall cause the hooked target to be inhibited from the display at the ETD console, but shall not erase the associated computer-stored data from the ETD display output file. In response to the suppress action, when hooked, the computer software shall cause the valid bit in the corresponding control word to be set equal to ZERO.
14, 15	ITR1 Code. These bits shall be used as shown in Figure 14 to uniquely identify the ETD to computer (ITR1) switch code format word.
16 through 25	Category Select. These bits shall be used to indicate the statuses of the ETD console DATA SELECT switches.

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Figure B8-17. ITR1 Word Content and Usage (Sheet 2 of 3)

Bit	Description
26	Delete. This bit shall be posted upon activation of the Delete switch on the ETD front panel. Activation of this function shall cause the hooked datum to be removed from the display and from the display buffer.
27	Spare.
28	Last Word/Next-to-Last Word. This bit shall be posted in conjunction with a light pen hooking operation and used to indicate to the computer whether the character being light pen-hooked was displayed from the last word transmitted to the ETD or the next-to-last word transmitted. The computer software shall use this bit to tag the proper control word/data word set in the display output file as the display data group hooked by the ETD.
29	Light Pen. This bit shall identify the feedback message as containing valid light pen data. The light pen bit shall be posted in the first ITR word transmitted to the computer as the result of a light pen interrupt indicator sequence and shall cause the computer to reset the keyword counter and reinitiate transmission of the display output file via on OFR word.
30	Test. This bit shall be used to request output of a computer-generated test pattern. The computer software shall cause the normal display output file to be replaced by a limited test pattern file, when the test bit is equal to one. The contents of the test pattern file shall be sufficient to exercise the total ETD symbol/character library and to verify the vector/line processing capability of the ETD. Deactivation of the ETD TEST switch on the front panel of the ETD shall cause the normal display output file to be transmitted from the computer.
31	Parity Error. This bit shall be posted when the ETD detects a Parity Error.

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Figure B8-17. ITR1 Word Content and Usage (Sheet 3 of 3)

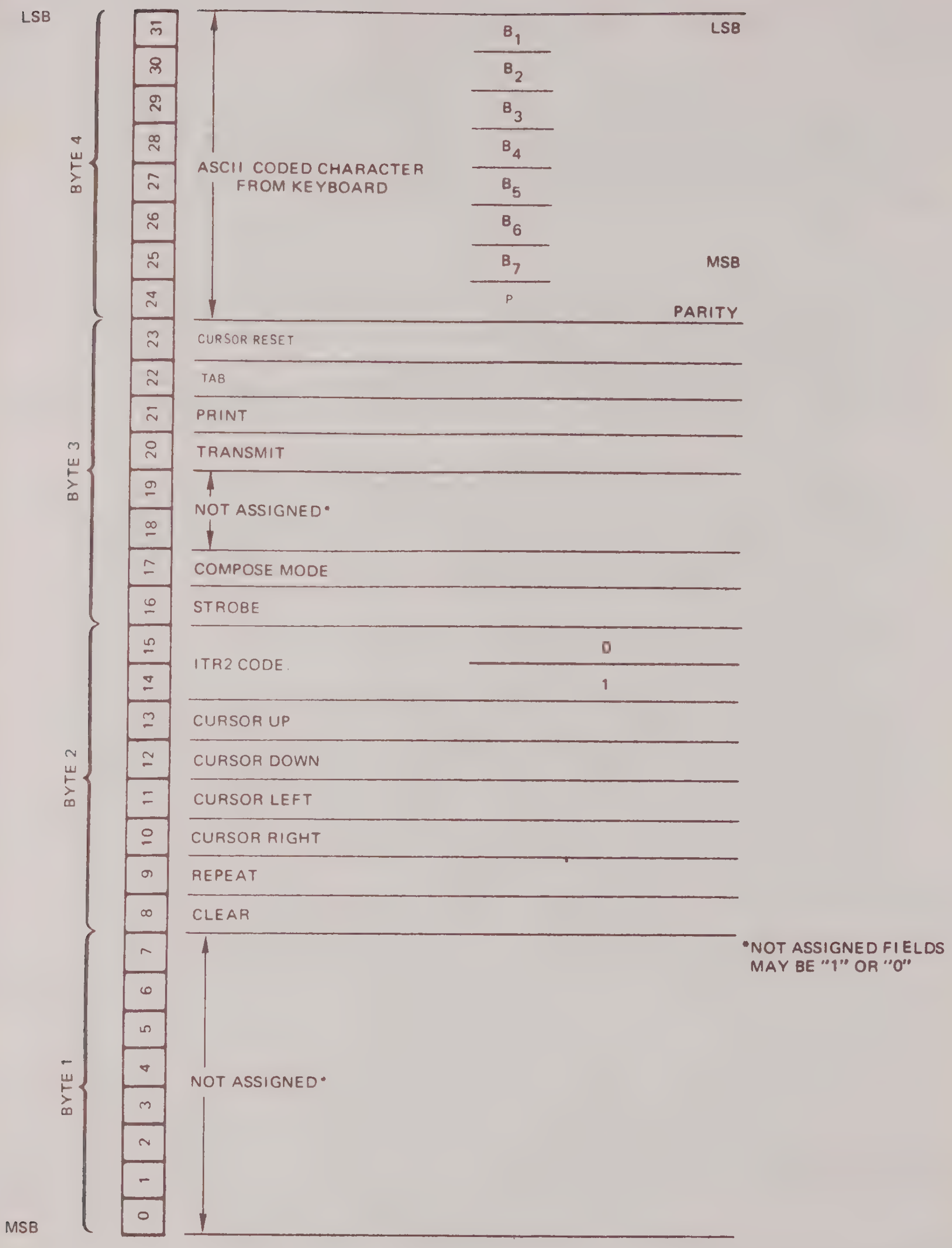
LSB
MSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
ASCII CODED CHARACTER FROM KEYBOARD
B1
B2
B3
B4
B5
B6
B7
P
LSB
MSB
PARITY
CURSOR RESET
TAB
PRINT
TRANSMIT
NOT ASSIGNED*
COMPOSE MODE
STROBE
ITR2 CODE
0
1
CURSOR UP
CURSOR DOWN
CURSOR LEFT
CURSOR RIGHT
REPEAT
CLEAR
NOT ASSIGNED*
*NOT ASSIGNED FIELDS MAY BE "1" OR "0"

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Figure B8-18. ETD-to-Computer ITR No. 2, Keyboard Code Format

Bit	Description
0 through 7	Not assigned.
8	Clear. This bit indicates that a pulse was received from the ETD keyboard in response to the CLEAR switch having been pressed. This 1.5 ±0.5 microsecond, debounced pulse does not occur more than once per ETD display cycle. This bit is posted for one and only one ITR sequence for each pulse received.
9	Repeat. This bit indicates that the ETD keyboard REPEAT switch is pressed.
10	Cursor right. This bit indicates that the ETD keyboard CURSOR → (right) switch is pressed.
11	Cursor left. This bit indicates that the ETD keyboard CURSOR ← (left) switch is pressed.
12	Cursor down. This bit indicates that the ETD keyboard CURSOR ↓ (down) switch is pressed.
13	Cursor up. This bit indicates that the ETD keyboard CURSOR ↑ (up) switch is pressed.
14, 15	ITR2 code. These bits are used as shown in figure 2-14 to uniquely identify the ETD to computer (ITR2) keyboard code format word.
16	Strobe. This bit indicates that a pulse was received from the ETD keyboard in response to the STROBE switch having been pressed. This 1.5 ±0.5 microsecond, debounced pulse does not occur more than once per ETD display cycle. This bit is posted for one and only one ITR sequence for each pulse received.
17	Compose mode. This bit indicates that keyboard COMPOSE switch is pressed.
18, 19	Not used.
20	Transmit. This bit indicates that a pulse was received from the ETD keyboard in response to the XMIT (transmit) switch having been pressed. This 1.5 ±0.5 microsecond, debounced pulse does not occur more than once per ETD display cycle. This bit is posted for one and only one ITR sequence for each pulse received.

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Figure B8-19. ITR2 Word Content and Usage (Sheet 1 of 2)

Bit	Description
21	Print. This bit indicates that the PRINT control on the ETD keyboard is activated and used in conjunction with the transmit control to direct ETD keyboard data via the CPU to the medium-speed printer (MSP).
22	Tab. This bit indicates that a pulse was received from the ETD keyboard in response to the TAB switch having been pressed. This 1.5 ±0.5 microsecond, debounced pulse does not occur more than once per ETD display cycle. This bit is posted for one and only one ITR sequence for each pulse received.
23	Cursor reset. This bit indicates that a pulse was received from the ETD keyboard in response to the CURSOR RESET switch having been pressed. This 1.5 ±0.5 microsecond, debounced pulse does not occur more than once per ETD display cycle. This bit is posted for one and only one ITR sequence for each pulse received.
24	Parity. This bit is generated by the ETD keyboard and transmitted to the CPU along with each 7-bit ASCII code. Odd parity results when the 7-bit ASCII code and the parity bit are combined.
25 through 31	ASCII code. A 7-bit ASCII character code, as shown in figure 2-7, is sent to the CPU from the ETD keyboard as long as the data remains on the keyboard data lines.

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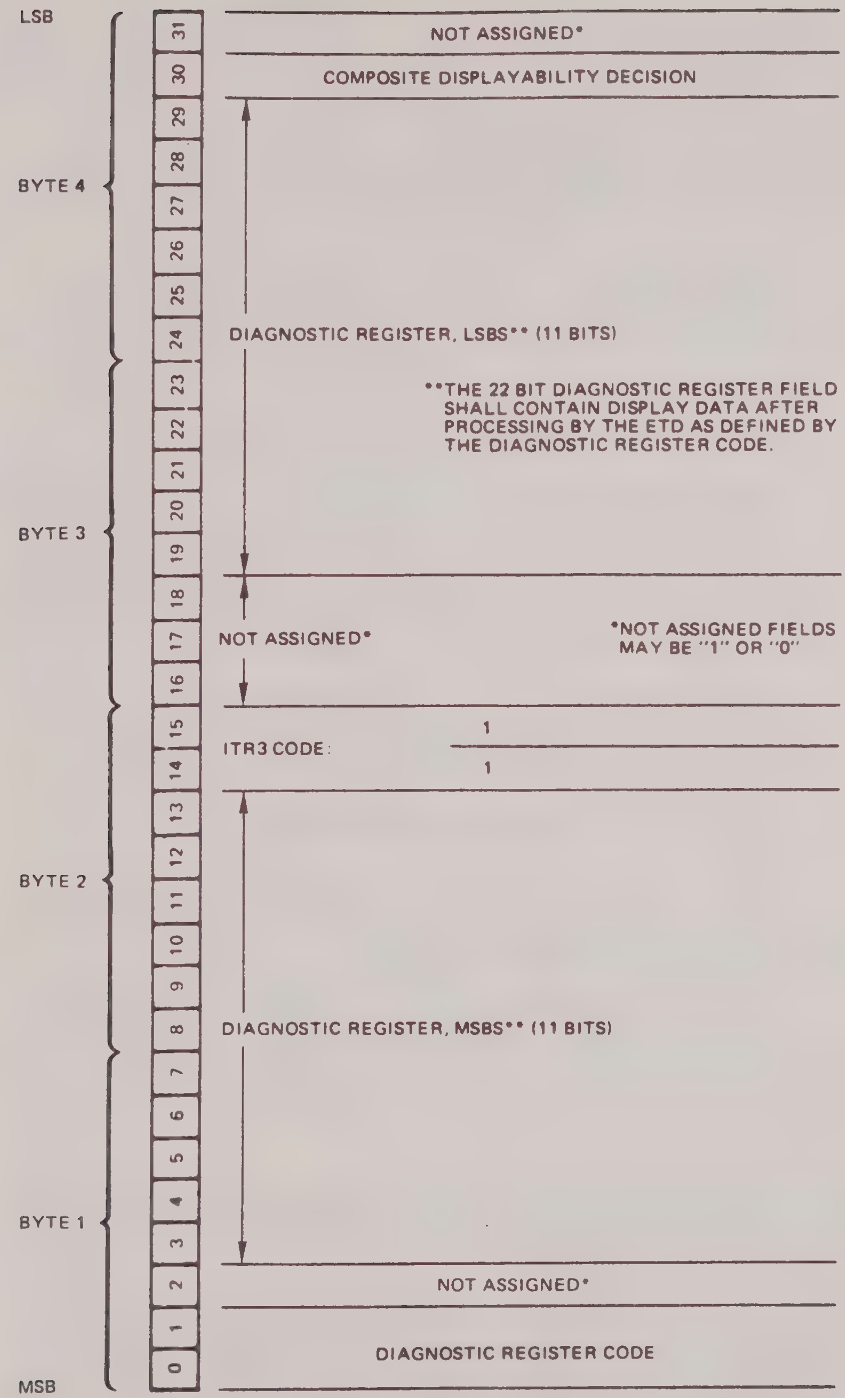
Figure B8-19. ITR2 Word Content and Usage (Sheet 2 of 2)


LSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
MSB
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
NOT ASSIGNED*
COMPOSITE DISPLAYABILITY DECISION
DIAGNOSTIC REGISTER, LSBS** (11 BITS)
NOT ASSIGNED*
ITR3 CODE:
1
1
DIAGNOSTIC REGISTER, MSBS** (11 BITS)
NOT ASSIGNED*
DIAGNOSTIC REGISTER CODE

**THE 22 BIT DIAGNOSTIC REGISTER FIELD SHALL CONTAIN DISPLAY DATA AFTER PROCESSING BY THE ETD AS DEFINED BY THE DIAGNOSTIC REGISTER CODE.

*NOT ASSIGNED FIELDS MAY BE "1" OR "0"

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Figure B8-20. ETD-to-Computer (ITR Format No. 3) Diagnostic Code Format

Bit	Description
0, 1	Diagnostic register code. The diagnostic register code corresponds identically to the code programmed into the OFR word via the diagnostic control software. The CPU interprets this code as follows: Code 0 0 Diagnostic Register 1: This code indicates to the CPU that the diagnostic register field contains the X-Y position values as defined at the registers driving the ETD position displays. 0 1 Diagnostic Register 2: This code indicates to the CPU that the diagnostic register field contains the X-Y vector values as defined at the register driving the ETD vector digilogs. 1 0 Diagnostic Register 3: This code indicates to the CPU that the 10 most significant bits of the diagnostic register field contain the character generator for the first character processed from the previous character word received. The 10 least significant bits of the diagnostic register field contain the 10 most significant bits stored in the ETD input register as a result of the last word transmitted from the CPU. 1 1 Diagnostic Register 4: This code indicates to the CPU that the diagnostic register field contains the 22 least significant bits stored in the ETD input register as a result of the last word transmitted from CPU.
2	Not assigned.
3 through 13	Diagnostic register, MSBS. This field contains the 11 most significant bits of the ETD diagnostic register. The contents of this field varies in accordance with the diagnostic register code.
14, 15	ITR3. These bits are used as shown in figure 2-15 to uniquely identify the ETD to computer (ITR3) diagnostic code format.
16 through 18	Not assigned.
19 through 29	Diagnostic register, LSBS. This field contains the 11 least significant bits of the ETD diagnostic register. The contents of this field varies in accordance with the diagnostic register code.
30	Composite displayability decision. This bit represents the status of the ETD Z-axis composite Z-axis control signal for the last word received and processed by the ETD. A ONE indicates that the data contained in the last word received from the ETD was displayable.
31	Not assigned.

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Figure B8-21. ITR3 Word Content and Usage

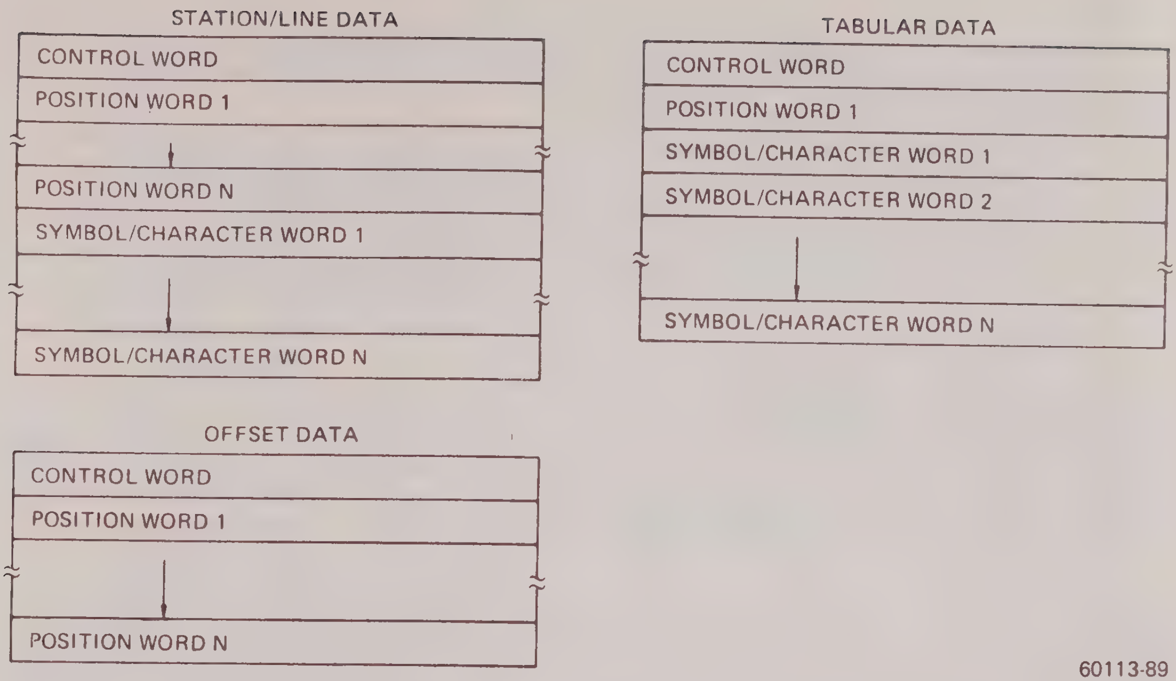
STATION/LINE DATA
CONTROL WORD
POSITION WORD 1
POSITION WORD N
SYMBOL/CHARACTER WORD 1
SYMBOL/CHARACTER WORD N
TABULAR DATA
CONTROL WORD
POSITION WORD 1
SYMBOL/CHARACTER WORD 1
SYMBOL/CHARACTER WORD 2
SYMBOL/CHARACTER WORD N
OFFSET DATA
CONTROL WORD
POSITION WORD 1
POSITION WORD N
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Figure B8-22. ETD Data Structures

Section IX. COMMUNICATIONS SECURITY INTERFACE NETWORK

B9-1. CSIN General

The communications security interface network (CSIN) provides the interface between the computer and the key generator (KG) which do the actual message encryption and decryption. The CSIN *does not* interface with the DDT's. The CSIN operates in a full duplex mode with the computer and therefore requires two I/O addresses.

B9-2. CSIN Capabilities

The CSIN basically supports data transfers at the rate required by the KG's.

B9-3. CSIN References

Computer Development Specification, EL-CP-0004-41101

B9-4. CSIN-to-Computer Interface

The CSIN can be more readily understood if it is viewed in terms of the real time clocks (RTC) in the computer. The CSIN is in the same basic category as an RTC and the computer interface is similar. The CSIN has two dedicated I/O addresses, as follows:

a. *I/O Address 06.* Used to input data to the computer and for all device commands and interrupts.

b. *I/O Address 07.* Used to output data from the computer.

All communication between computer and CSIN is on an 8-bit byte basis.

B9-5. CSIN Command and Control Word(s)

Control of the CSIN by the computer is via device command bytes. As previously mentioned the CSIN has separate addresses for input and output, however all control functions are routed via the input channel address 06. Figure B9-1 illustrates the device command byte format and figure B9-2 defines content and usage.

B9-6. CSIN Status Word(s)

Device status information is transferred to the computer from the CSIN in the form of an ITR word consisting of an 8-bit byte. The transfer is initiated on the input channel (address 06) when the computer issues an ITR control byte. The status information is placed in bits 24 through 31 of the register. The CSIN is designed

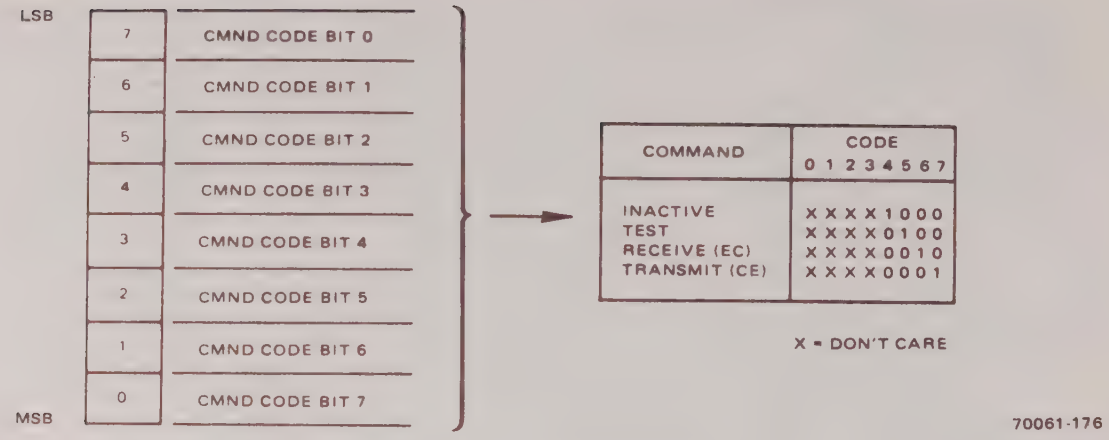
LSB
MSB
7
6
5
4
3
2
1
0
CMND CODE BIT 0
CMND CODE BIT 1
CMND CODE BIT 2
CMND CODE BIT 3
CMND CODE BIT 4
CMND CODE BIT 5
CMND CODE BIT 6
CMND CODE BIT 7
COMMAND
CODE
0 1 2 3 4 5 6 7
INACTIVE
TEST
RECEIVE (EC)
TRANSMIT (CE)
X X X X 1 0 0 0
X X X X 0 1 0 0
X X X X 0 0 1 0
X X X X 0 0 0 1
X = DON'T CARE
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Figure B9-1. CSIN Device Command Byte

Code	Description
0001	Transmit (CE) Mode - When the CSIN buffer recognizes a DEV CE command, the buffer will signal the KG to generate the sync pattern. This pattern will be input by the CSIN buffer on I/O Address 06. The buffer will then request the output of data on I/O Address 07 and send it to the KG for encoding. The encoded KG output will be input by the CSIN buffer on I/O Address 06.
0010	Receive (EC) Mode - When the CSIN buffer recognizes a DEV EC command, the buffer will request the output of data on I/O address 07 and send it to the KG for decoding. The decoded KG output will be input by the CSIN buffer on I/O Address 06.
0100	Test Mode - When the CSIN buffer recognizes a DEV Test command, the buffer will perform a loop test. The buffer will request the output of data on I/O address 07 and will input the same data on I/O address 06.
1000	Inactive Mode - When the CSIN buffer recognizes a DEV Inactive command, the buffer will reset all logic and enter an inactive state. The buffer will respond to ITR commands but will otherwise remain inactive until a new DEV command is received. (NOTE: In the EC or CE modes, all data transmissions, whether sync or message text, are seven bits plus parity. Data bit zero, the most significant bit of each byte will always be a zero. This is also true for transmissions in the test mode.)

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Figure B9-2. CSIN Command Code Content and Usage

to respond to an ITR command without any interference with its normal mode operation. Figure B9-3 illustrates the ITR Status Byte format and figure B9-4 defines content and usage.

B9-7. CSIN Interrupts

An interrupt is generated by the CSIN on input channel address 06 whenever one of the following conditions occur.

a. Parity Error on CPU Output Data.

b. KG Power Off.

c. KG Alarm.

d. KG Cable Disconnect.

No interrupt status byte is transferred with the interrupts, the device status must be ascertained via an ITR command. (See Special Considerations for more detailed error condition information.)

B9-8. CSIN Data Structure

Data is transferred between the computer and CSIN on a byte by byte basis with each byte representing an ASCII character (either straight or encrypted). There are no hardware limitations on the number of bytes/characters that may be transferred, only core requirements and system tolerances cause any limitations.

B9-9. CSIN Special Considerations

a. The result of various possible error conditions are defined as follows:

(1) *Parity Error on Commands or the Command Code Not Recognized.* The CSIN buffer will not send an acknowledge to the computer if either of these conditions occur. A device time out occurs and a jump to Program Level 2 is taken by the computer.

(2) *Parity Error on Computer Output Data.* The CSIN buffer will discontinue processing the message if this condition occurs. The buffer will send an interrupt to the computer on I/O Address 06. The buffer must be restarted with a new DEV command to continue processing.

(3) *KG Error.* The three KG error conditions which are detected by the CSIN buffer are KG Power Off, KG Alarm, and KG cable disconnected. The CSIN buffer will discontinue processing the message if any of these conditions occur. The buffer will send an interrupt to the computer on I/O Address 06. The buffer must be restarted with a new DEV command to continue processing. (NOTE: If the CSIN buffer receives a new DEV command and the error condition still exists another interrupt will be sent to the computer and the buffer will remain inactive.)

b. To facilitate more expedient program development the following suggestions are provided:

(1) When placing the CSIN buffer in the test mode, set the block length for I/O Address 06 equal to the number of bytes in the test message. Set the block length for I/O Address 07 equal to at least two greater than this number to prevent an EOB on I/O Address 07 from terminating the CSIN buffer operation before the last byte is input to the computer on I/O Address 06.

(2) When placing the CSIN buffer in the receive (EC) mode, set the block length for I/O Address 06 equal to the number of bytes in the message text. Set the block length for I/O Address 07 equal to at least two greater than the number of bytes in the message text plus the number of bytes in the sync pattern.

(3) When placing the CSIN buffer in the transmit (CE) mode, set the block length for I/O Address 06 equal to the number of bytes in the message text plus the number of bytes in the sync pattern. Set the block length for I/O Address 07 equal to at least two greater than the number of bytes in the message text.

(4) As an added precaution to ensure that a message has been encrypted correctly, an ITR command should be sent to the CSIN buffer upon the completion of message processing in the transmit (CE) mode. The program should check that the FO status bit in termination word is a one and that all other status bits are zero.

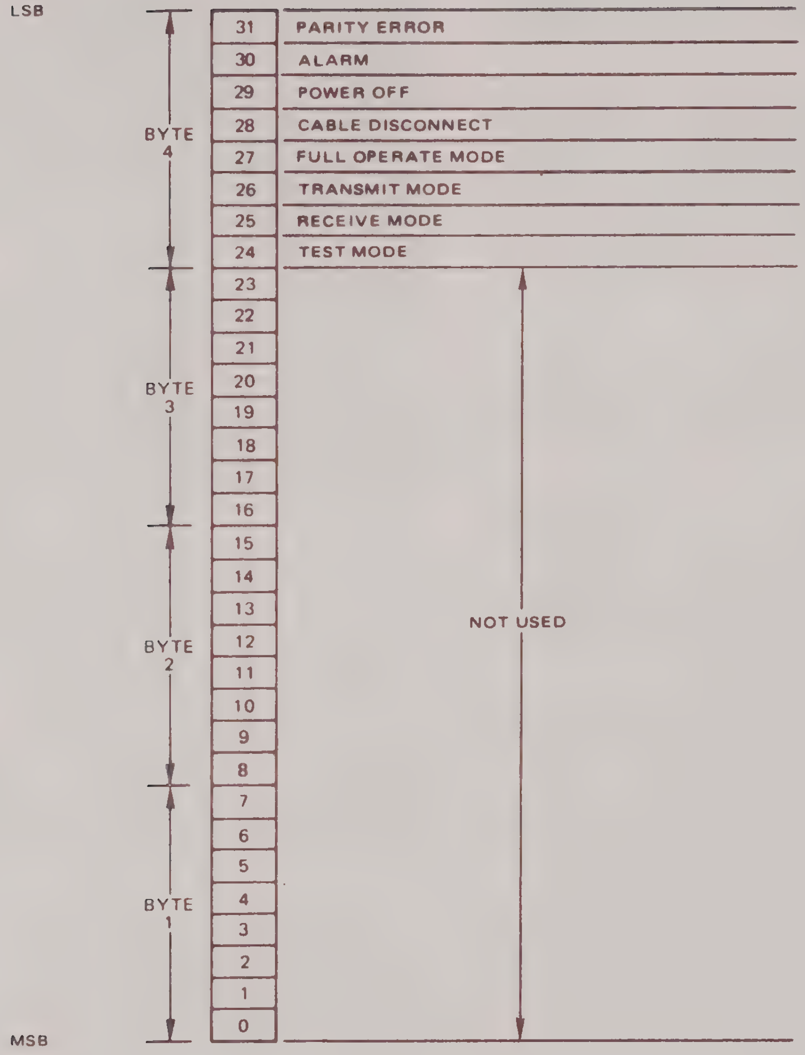
LSB
BYTE 4
31 PARITY ERROR
30 ALARM
29 POWER OFF
28 CABLE DISCONNECT
27 FULL OPERATE MODE
26 TRANSMIT MODE
25 RECEIVE MODE
24 TEST MODE
BYTE 3
23
22
21
20
19
18
17
16
BYTE 2
15
14
13
12
11
10
9
8
BYTE 1
7
6
5
4
3
2
1
0
NOT USED
MSB

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Figure B9-3. CSIN ITR Word

Bit	Description
0 through 23	Not used.
24	Test mode. This bit is set when a DEV Test Command is received and is reset when any other DEV command or an EOB command is received.
25	Receive mode. This bit is set when a DEV EC command is received and is reset when any other DEV command or an EOB command is received.
26	The CSIN buffer is in the transmit (CE) mode. This bit is set when a DEV CE command is received and is reset when any other DEV command or an EOB command is received.
27	Full operate mode. This bit is set when a previously false full operate signal is received from the KG and the CSIN buffer is in the EC or CE modes. This bit is reset when the KG full operate signal goes false or when the CSIN buffer receives another DEV command. (NOTE: The full operate signal from the KG indicates that the KG has recognized the sync pattern in a receive message (EC mode) or has generated the sync pattern in a transmit message (CE mode).)
28	Cable disconnect. The CSIN buffer has detected that one or more of the cables to the KG is disconnected. This bit is set as long as the condition exists.
29	Power off. The CSIN buffer has detected that the KG power has not been turned on. This bit is set as long as the condition exists.
30	Alarm. The CSIN buffer has detected a KG error alarm signal. This bit is set as long as the condition exists.
31	Parity error. The CSIN buffer has detected a parity error when receiving the last data output on I/O Address 07. This bit is set when the parity error occurs and is reset after the status byte is sent to the computer in response to an ITR command.

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Figure B9-4. CSIN ITR Word Content and Usage

Section X. SYSTEM INTERFACE UNIT

B10-1. SIU General

The system interface unit (SIU) is a special purpose device designed to allow communications between the AN/GYK-12 and the PDP-11 controlled smart peripheral system (SPS). The SIU provides for bootstrap loading of the AN/GYK-12 from the SPS and half duplex transfers of data blocks between AN/GYK-12 and the SPS. The following information is germain only to the AN/GYK-12 side of the SIU interface.

B10-2. SIU Capabilities

The SIU can be controlled, provide status about itself, and support data transfers like any other peripheral device. Data transfers are at the maximum rate possible from the AN/GYK-12 IOX.

B10-3. SIU References

Not applicable

B10-4. SIU-to-Computer Interface

Data transfers between the SIU and AN/GYK-12 are performed on an automatic input/output and interrupt basis. Communication is via bytes and words with actual data transfers being accomplished on a 8-bit byte basis using the information lines. Figure B10-1 illustrates the various interface lines.

B10-5. SIU Command Control Word(s)

Control of the SIU from the AN/GYK-12 is via device command bytes. Figure B10-2 illustrates the format and figure B10-3 defines contents and usage.

B10-6. SIU Status Word(s)

When an ITR command is issued from the computer (ITR instruction is executed). Device status is returned to the computer from the SIU, in the form of an ITR word consisting of four 8-bit bytes, figure B10-4 illustrates the ITR word format and figure B10-5 defines content and usage.

B10-7. SIU Interrupts

The SIU generated interrupt to the AN/GYK-12 is used to transfer status from the SIU. The interrupt sequence occurs for one of the following reasons and causes the interrupt status byte to be transferred.

a. A parity error is detected during an automatic output operation.

b. SPS Word Count Register has counted to zero before an EOB is received.

c. An interrupt 6 or 7 command is set via the SPS software.

d. As a result of a normal EOB sequence.

Figure B10-6 illustrates the interrupt byte format and figure B10-7 defines its content and usage. (It should be noted that the data is the same as in the ITR status word.)

B10-8. SIU Data Structure

No specific restrictions are placed on the contents of the data transferred between SIU and computer. However, to maximize core usage and SPS disk storage, data buffers should be organized on a 32-bit word basis.

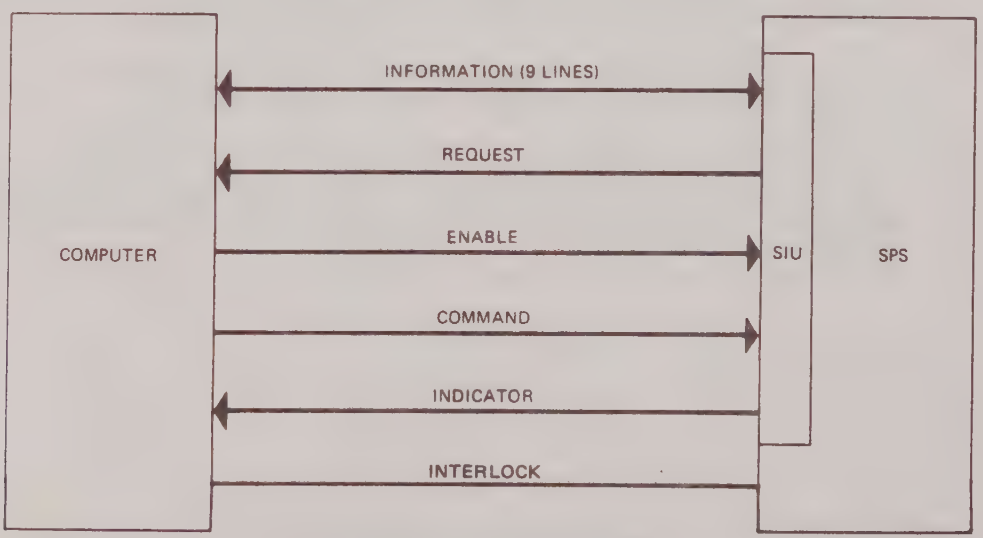
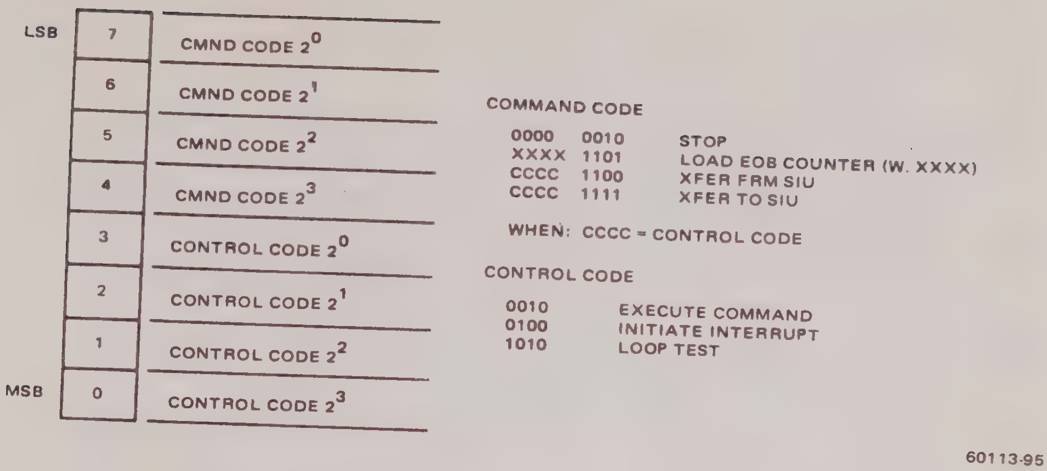


Figure B10-1. SIU Interface Lines



	Bit	
LSB	7	CMND CODE 2^0
	6	CMND CODE 2^1
	5	CMND CODE 2^2
	4	CMND CODE 2^3
	3	CONTROL CODE 2^0
	2	CONTROL CODE 2^1
	1	CONTROL CODE 2^2
MSB	0	CONTROL CODE 2^3

COMMAND CODE

0000	0010	STOP
XXXX	1101	LOAD EOB COUNTER (W. XXXX)
CCCC	1100	XFER FRM SIU
CCCC	1111	XFER TO SIU

WHEN: CCCC = CONTROL CODE

CONTROL CODE

0010	EXECUTE COMMAND
0100	INITIATE INTERRUPT
1010	LOOP TEST

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Figure B10-2. SIU Device Command Format

Code	Description
0010	Stop -
1101	Load EOB Counter - Loads counter with upper four bits of DEV COMMAND byte. Used to indicate the number of EOB control bytes to be ignored when data transfers of more than 2048 words are required. Range - 0 to 16.
1100	Transfer from SIU - Indicates data is to be transfered from the SIU to the AN/GYK-12.
1111	Transfer to SIU - Indicates data is to be transferred to the SIU from the AN/GYK-12.
0010	Execute Command - The SIU shall start transferring data as specified by the command, either Transfer To SIU or Transfer From SIU.
0100	Initiate Interrupt - The SIU causes an interrupt to the PDP-11 system and shall set the CIF bit in the DR-11B STATUS Register (DRST). The DRST is accessable by the PDP-11 only. Reset on EOB or SIU Reset. C = 0: No interrupt is generated and the CIF bit in the DRST is not set.
1010	Loop Test - The SIU shall set the Test F/F within the SIU, which, when set, shall allow the AN/GYK-12 to conduct a loop test to the SIU. The loop test will store data in the SIU with a Transfer To SIU command and read it back with a Transfer From SIU command.

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Figure B10-3. Command Code Content and Usage

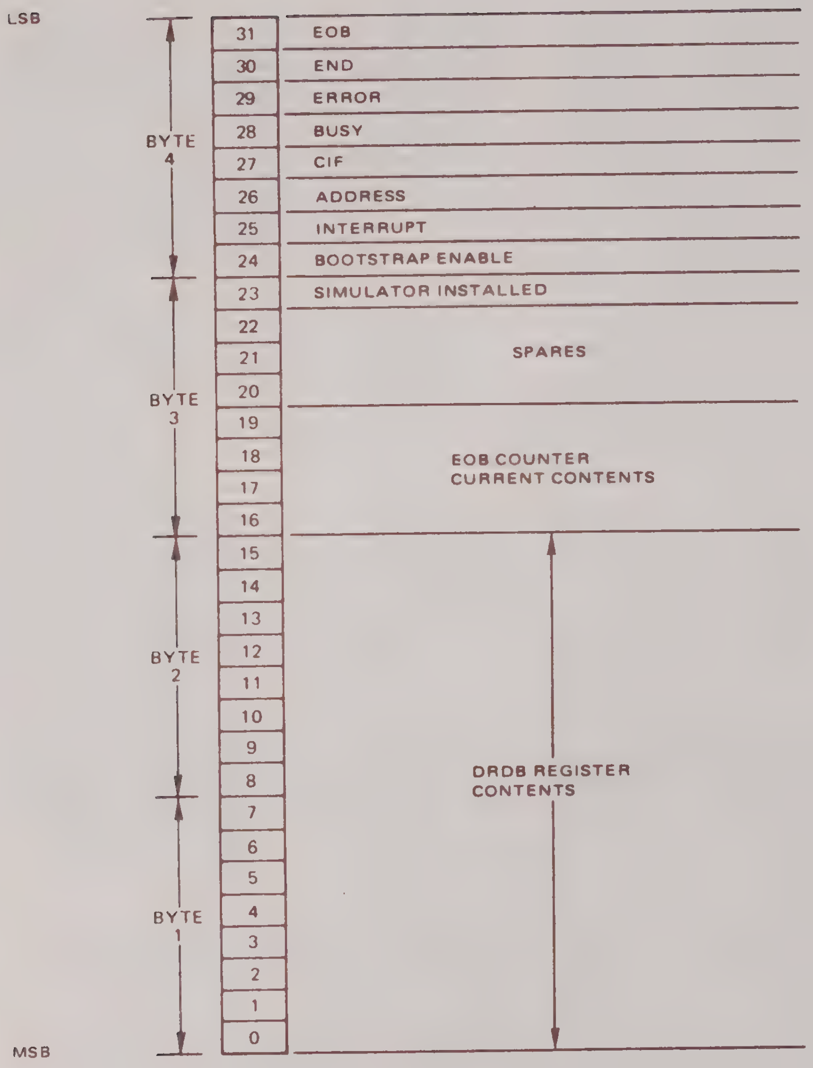
LSB
MSB
BYTE 4
BYTE 3
BYTE 2
BYTE 1
31
30
29
28
27
26
25
24
23
22
21
20
19
18
17
16
15
14
13
12
11
10
9
8
7
6
5
4
3
2
1
0
EOB
END
ERROR
BUSY
CIF
ADDRESS
INTERRUPT
BOOTSTRAP ENABLE
SIMULATOR INSTALLED
SPARES
EOB COUNTER CURRENT CONTENTS
DRDB REGISTER CONTENTS

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Figure B10-4. SIU ITR Word Format

Bit	Description
0-15	DRDB - Bits 0-15 shall contain the contents of the DR-11B Data Buffer Register (DRDB) which is loaded under PDP-11 software control. This field shall be used in conjunction with the Function Bits 01-03 of the DR-11B Status Register (see TABLE IV) to pass control information from the PDP-11 to the AN/GYK-12 computer.
16-19	EOB Counter - Bits 16-19 shall contain the present contents of the SIU EOB counter.
20-22	Spare bits shall always be zeros in the returned ITR.
23	DR-11-B simulator installed.
24	Bootstrap Enable (BE) shall be set by the PDP-11 software. When BE = 1 the SIU shall accept commands on device channel '11' but when BE = 0 the SIU shall ignore all commands in channel '11'. Reset by PDP-11 software.
25	Interrupt (INT) shall be set by the PDP-11 software to cause an interrupt to the AN/GYK-12 to inform the AN/GYK-12 that the PDP-11 has a request to be serviced. Reset at the end of the Interrupt sequence.
26	Address (ADD) shall specify on which channel the programmed operation is to take place. ADD = 0 shall indicate address 6 and ADD = 1 shall indicate address 7.
27	Control Information Flag (CIF) shall indicate that the CIF F/F in the SIU has been set by the AN/GYK-12 software. The CIF F/F shall set the CIF bit (DRST bit 11) and the ATTN bit 1 (DRST bit 13) in the DR-11B see Figure 4, and initiate an interrupt to the PDP-11 system. Reset on normal EOB Termination or SIU reset.
28	The BUSY bit shall indicate that the SIU BUSY F/F is set. The BUSY F/F shall set the BUSY bit, DRST Bit 10 (Figure 4), to indicate that a data transfer or PDP-11 Interrupt is in process. Reset by a normal EOB, Error Interrupt, or SIU Reset.
29	The Error (ERR) bit shall indicate that an error has been detected in the interface. The Error F/F shall cause interrupts to occur on both the AN/GYK-12 and PDP-11 systems. Reset by Error Reset or SIU Reset from PDP-11. Sets PE bit DRST Bit 09 in the DR-11B (see Figure 4).
30	The END bit shall indicate that the PDP-11 Word Count Register DRWC has counted to zero.
31	The EOB bit shall indicate that the SIU EOB counter has counted to zero.

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Figure B10-5. SIU ITR Word Content and Usage

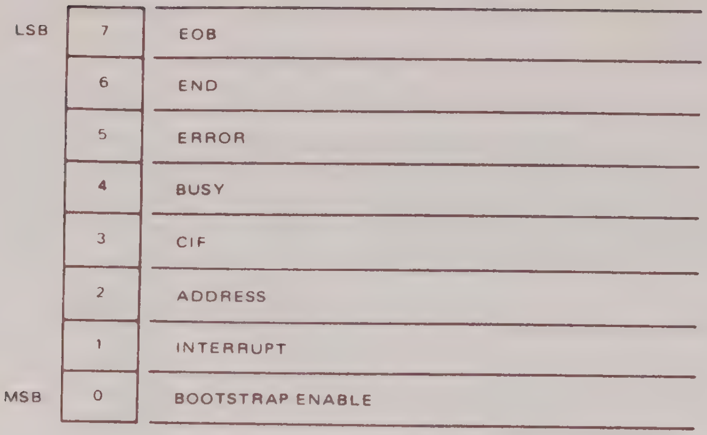

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Figure B10-6. SIU Interrupt Byte Format

Bit	Description
0	Bootstrap Enable (BE) shall be set by the PDP-11 software. When BE = 1 the SIU shall accept commands on device channel '11' but when BE = 0 the SIU shall ignore all commands in channel '11'. Reset by PDP-11 software.
1	Interrupt (INT) shall be set by the PDP-11 software to cause an interrupt to the AN/GYK-12 to inform the AN/GYK-12 that the PDP-11 has a request to be serviced. Reset at the end of the Interrupt sequence.
2	Address (ADD) shall specify on which channel the programmed operation is to take place. ADD = 0 shall indicate address 6 and ADD = 1 shall indicate address 7.
3	Control Information Flag (CIF) shall indicate that the CIF F/F in the SIU has been set by the AN/GYK-12 software. Reset on normal EOB Termination or SIU reset.
4	The BUSY bit shall indicate that the SIU Busy F/F is set. The BUSY F/F shall indicate that a data transfer or PDP-11 Interrupt is in process. Reset by a normal EOB, Error Interrupt, or SIU Reset.
5	The Error (ERR) bit shall indicate that an error has been detected in the interface. The Error F/F shall cause interrupts to occur on both the AN/GYK-12 and PDP-11 systems. Reset by Error Reset or SIU Reset from PDP-11.
6	The END bit shall indicate that the PDP-11 Word Count Register DRWC has counted to zero.
7	The EOB bit shall indicate that the SIU EOB counter has counted to zero.

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Figure B10-7. SIU Interrupt Byte Content and Usage

	PROCESS REGISTERS																																									
	IN▪R	IN LOC	INDEX REGISTERS													MASK	TRAP	PAGE CONTROL AND ADDRESS REGISTERS																PRIV & LEVEL LINK	QUEUE REGISTER	NOTE			NOT RELATED TO PROGRAM LEVELS			
LOCATION	00	01	02 03	04 05	06 07	08 09	0A 0B	0C 0D	0E 0F	10 11	12 13	14 15	16 17	18 19	1A 1B	1C 1D	1E 1F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	30 31	32 33	34 35	36	37	38 39	3A 3B	3C 3D	3E 3F
																																				COMMON REGISTERS						
LEVEL 0 0000	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	00	00	Q	E		PROGRAM ACTIVITY REGISTERS			
LEVEL 1 0040	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 01	LEVEL 01				K02	T02	K03	T03
LEVEL 2 0080	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 02	LEVEL 02				K04	T04	K05	T05
LEVEL 3 00C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 03	LEVEL 03				K06	T06	K07	T07
LEVEL 4 0100	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 04	LEVEL 04				K08	T08	K09	T09
LEVEL 5 0140	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 05	LEVEL 05				K10	T10	K11	T11
LEVEL 6 0180	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 06	LEVEL 06				K12	T12	K13	T13
LEVEL 7 01C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 07	LEVEL 07				K14	T14	K15	T15
LEVEL 8 0200	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 08	LEVEL 08				K16	T16	K17	T17
LEVEL 9 0240	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 09	LEVEL 09				K18	T18	K19	T19
LEVEL 10 0280	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 10	LEVEL 10				K20	T20	K21	T21
LEVEL 11 02C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 11	LEVEL 11				K22	T22	K23	T23
LEVEL 12 0300	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 12	LEVEL 12				K24	T24	K25	T25
LEVEL 13 0340	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 13	LEVEL 13				K26	T26	K27	T27
LEVEL 14 0380	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 14	LEVEL 14				K28	T28	K29	T29
LEVEL 15 03C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 15	LEVEL 15				K30	T30	K31	T31
LEVEL 16 0400	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 16	LEVEL 16				K32	T32	K33	T33
LEVEL 17 0440	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 17	LEVEL 17				K34	T34	K35	T35
LEVEL 18 0480	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 18	LEVEL 18				K36	T36	K37	T37
LEVEL 19 04C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 19	LEVEL 19				K38	T38	K39	T39
LEVEL 20 0500	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 20	LEVEL 20				K40	T40	K41	T41
LEVEL 21 0540	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 21	LEVEL 21				K42	T42	K43	T43
LEVEL 22 0580	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 22	LEVEL 22				K44	T44	K45	T45
LEVEL 23 05C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 23	LEVEL 23				K46	T46	K47	T47
LEVEL 24 0600	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 24	LEVEL 24				K48	T48	K49	T49
LEVEL 25 0640	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 25	LEVEL 25				K50	T50	K51	T51
LEVEL 26 0680	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 26	LEVEL 26				K52	T52	K53	T53
LEVEL 27 06C0	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 27	LEVEL 27				K54	T54	K55	T55
LEVEL 28 0700	0		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 28	LEVEL 28				K56	T56	K57	T57
LEVEL 29																																										

K = KEYWORD, T = TERMINATION WORD, Q = QUERY REGISTER, E = EXECUTIVE LINK REGISTER.

LEVEL 30 0780	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 30	LEVEL 30				K60	T60	K61	T61
LEVEL 31 07C0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 31	LEVEL 31				K62	T62	K63	T63
LEVEL 32 0800	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 32	LEVEL 32				K64	T64	K65	T65
LEVEL 33 0840	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 33	LEVEL 33				K66	T66	K67	T67
LEVEL 34 0880	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 34	LEVEL 34				K68	T68	K69	T69
LEVEL 35 08C0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 35	LEVEL 35				K70	T70	K71	T71
LEVEL 36 0900	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 36	LEVEL 36				K72	T72	K73	T73
LEVEL 37 0940	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 37	LEVEL 37				K74	T74	K75	T75
LEVEL 38 0980	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 38	LEVEL 38				K76	T76	K77	T77
LEVEL 39 09C0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 39	LEVEL 39				K78	T78	K79	T79
LEVEL 40 0A00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 40	LEVEL 40				K80	T80	K81	T81
LEVEL 41 0A40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 41	LEVEL 41				K82	T82	K83	T83
LEVEL 42 0A80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 42	LEVEL 42				K84	T84	K85	T85
LEVEL 43 0AC0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 43	LEVEL 43				K86	T86	K87	T87
LEVEL 44 0B00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 44	LEVEL 44				K88	T88	K89	T89
LEVEL 45 0B40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 45	LEVEL 45				K90	T90	K91	T91
LEVEL 46 0B80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 46	LEVEL 46				K92	T92	K93	T93
LEVEL 47 0BC0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 47	LEVEL 47				K94	T94	K95	T95
LEVEL 48 0C00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 48	LEVEL 48				K96	T96	K97	T97
LEVEL 49 0C40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 49	LEVEL 49				K98	T98	K99	T99
LEVEL 50 0C80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 50	LEVEL 50				K100	T100	K101	T101
LEVEL 51 0CC0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 51	LEVEL 51				K102	T102	K103	T103
LEVEL 52 0D00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 52	LEVEL 52				K104	T104	K105	T105
LEVEL 53 0D40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 53	LEVEL 53				K106	T106	K107	T107
LEVEL 54 0D80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 54	LEVEL 54				K108	T108	K109	T109
LEVEL 55 0DC0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 55	LEVEL 55				K110	T110	K111	T111
LEVEL 56 0E00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 56	LEVEL 56				K112	T112	K113	T113
LEVEL 57 0E40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 57	LEVEL 57				K114	T114	K115	T115
LEVEL 58 0E80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 58	LEVEL 58				K116	T116	K117	T117
LEVEL 59 0EC0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 59	LEVEL 59				K118	T118	K119	T119
LEVEL 60 0F00	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 60	LEVEL 60				K120	T120	K121	T121
LEVEL 61 0F40	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 61	LEVEL 61				K122	T122	K123	T123
LEVEL 62 0F80	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 62	LEVEL 62				K124	T124	K125	T125
LEVEL 63 0FC0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	LEVEL 63	LEVEL 63				K126	T126	K127	T127

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Figure FO-1. AN/GYK-12 Computer Special Registers Memory Map